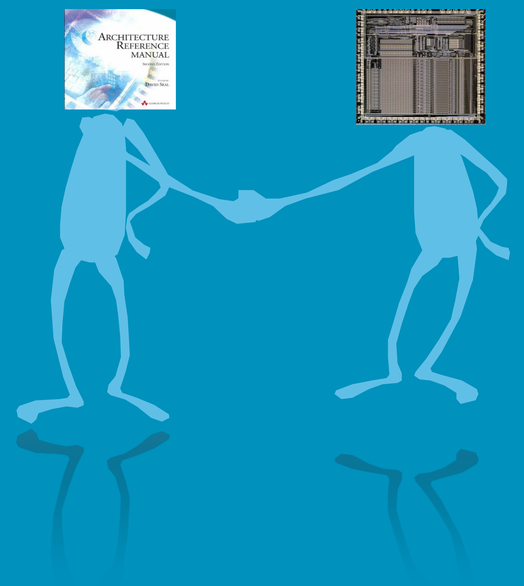
arm



Engineering Formal Specifications of the Arm Processor Architecture

Alastair Reid

Arm Research

@alastair_d_reid

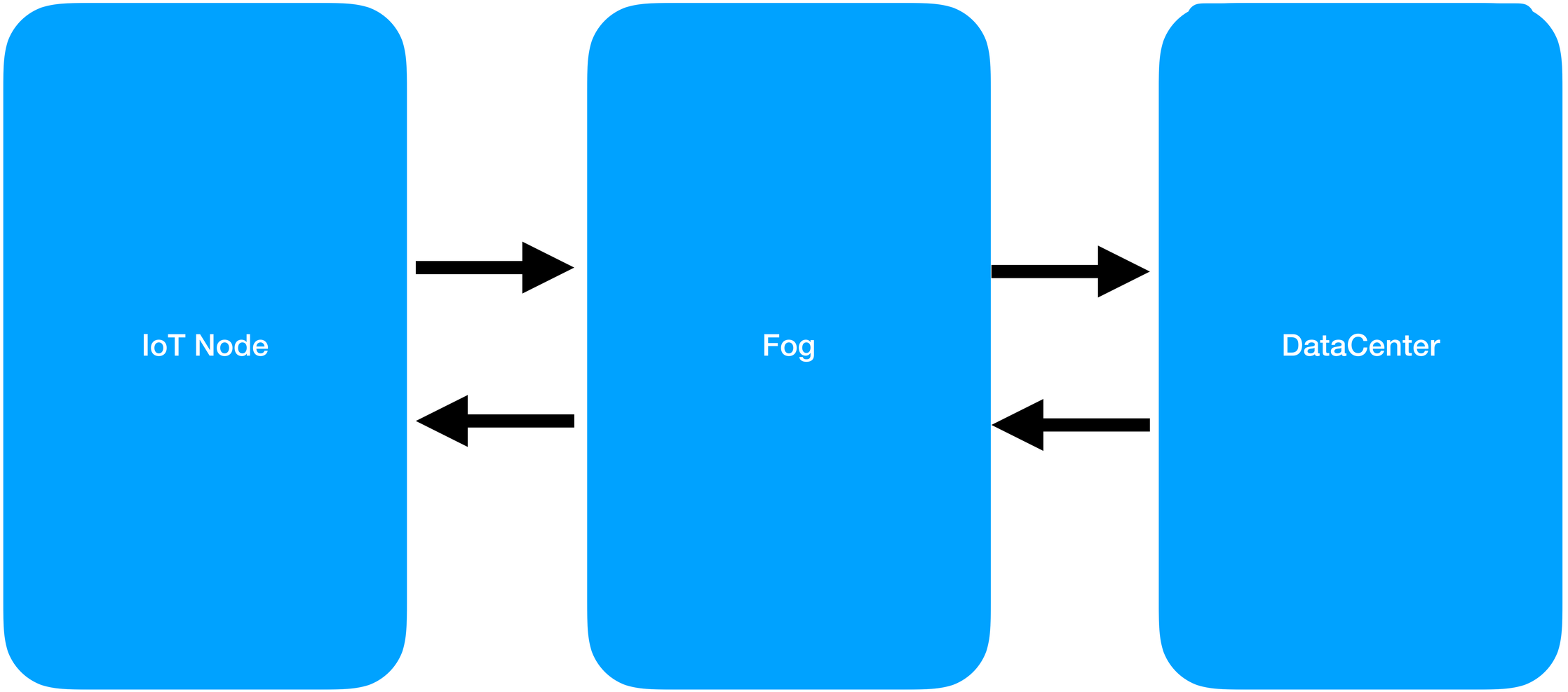
Engineering (Wikipedia)

Engineering is the creative application of science, mathematical methods, and empirical evidence

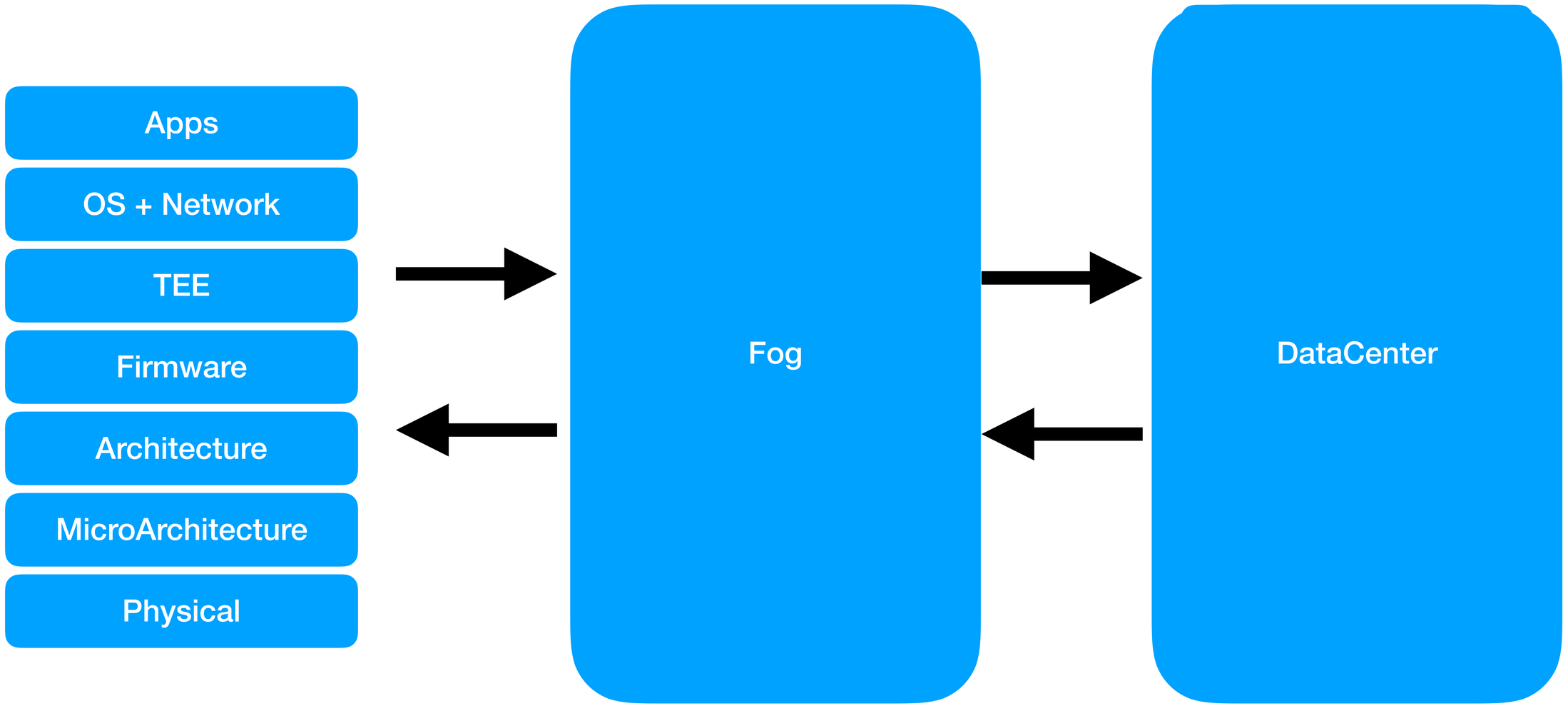
to the innovation, design, construction, operation and maintenance of structures, machines, materials, devices, systems, processes, and organizations

for the benefit of humankind.

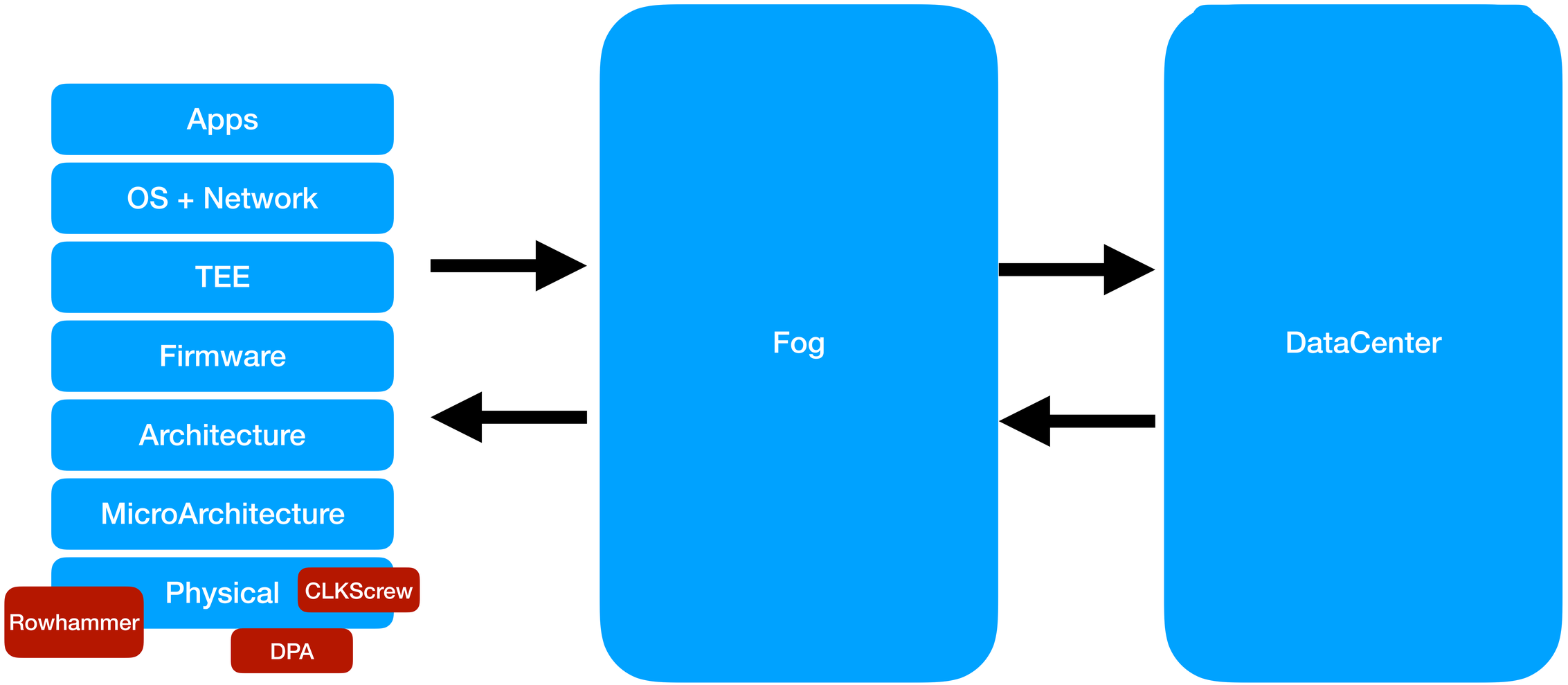
The IoT security problem



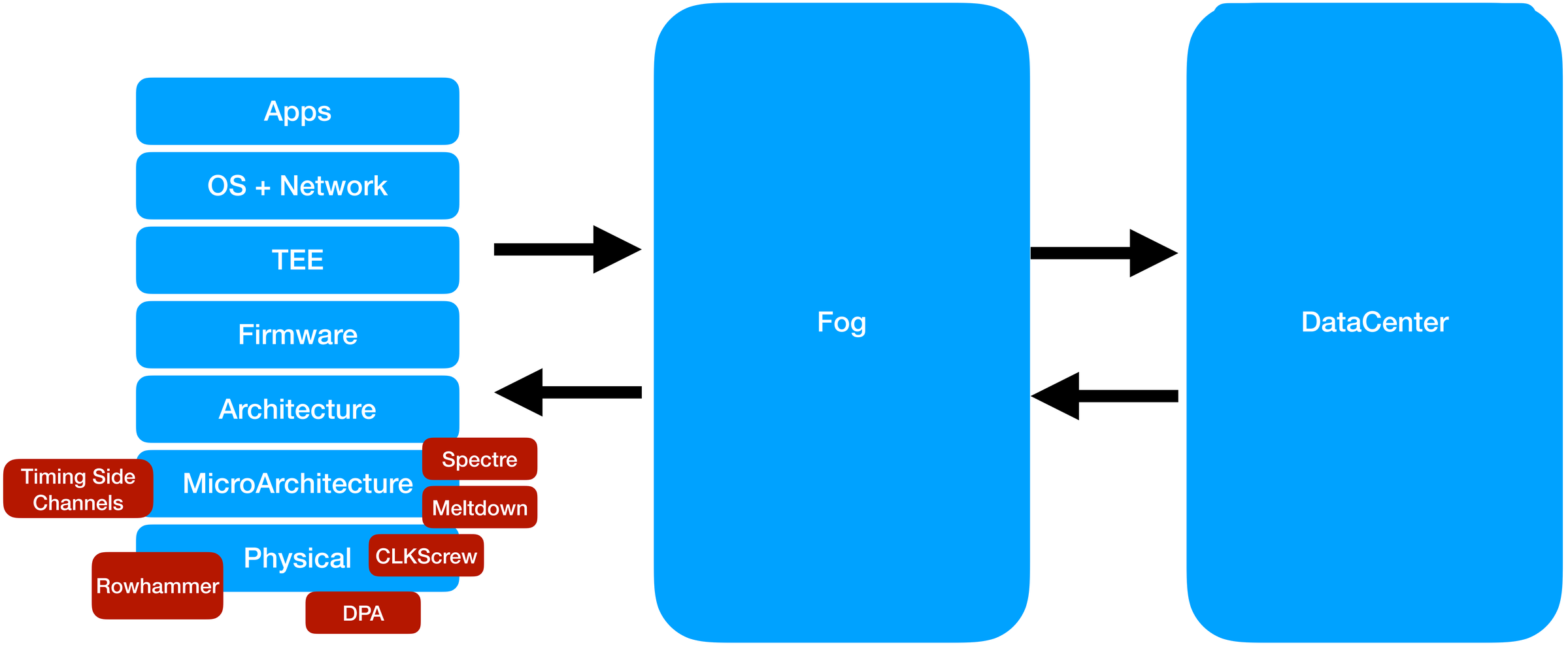
The IoT security problem



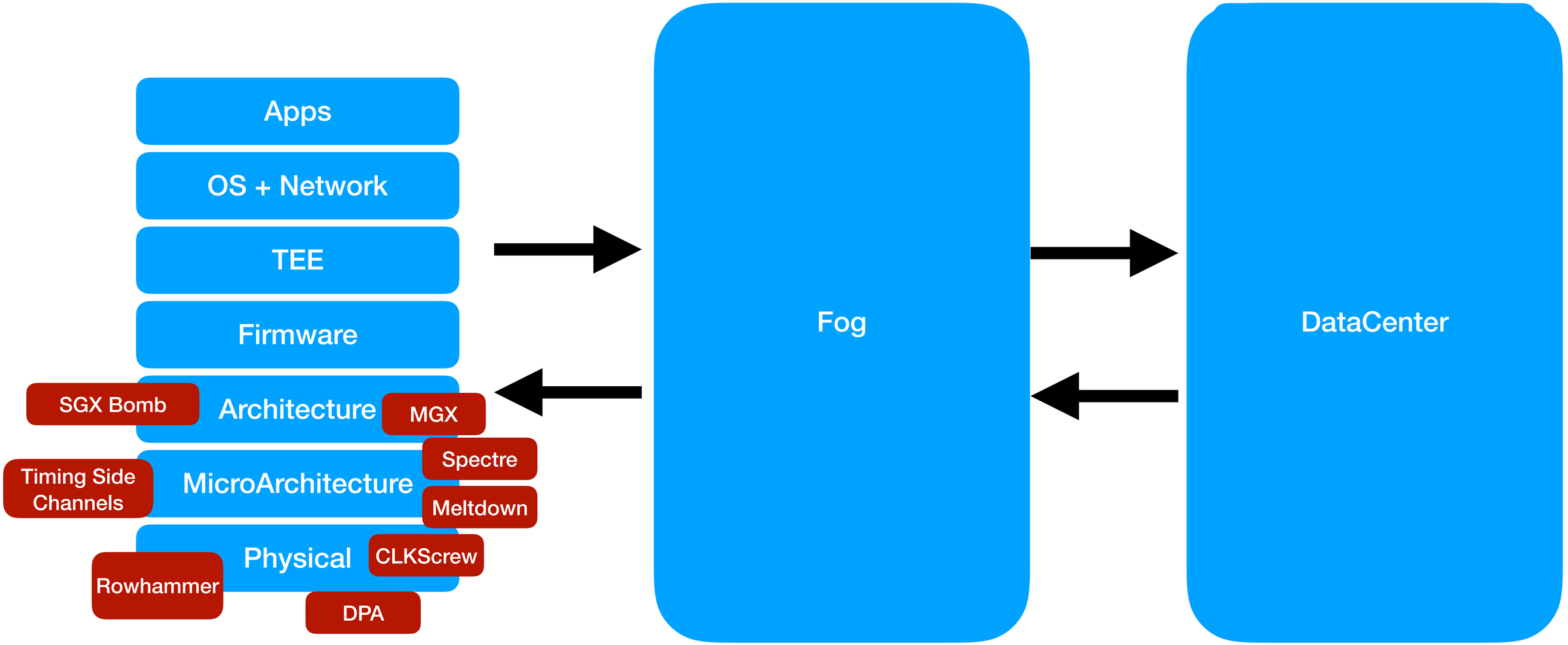
The IoT security problem



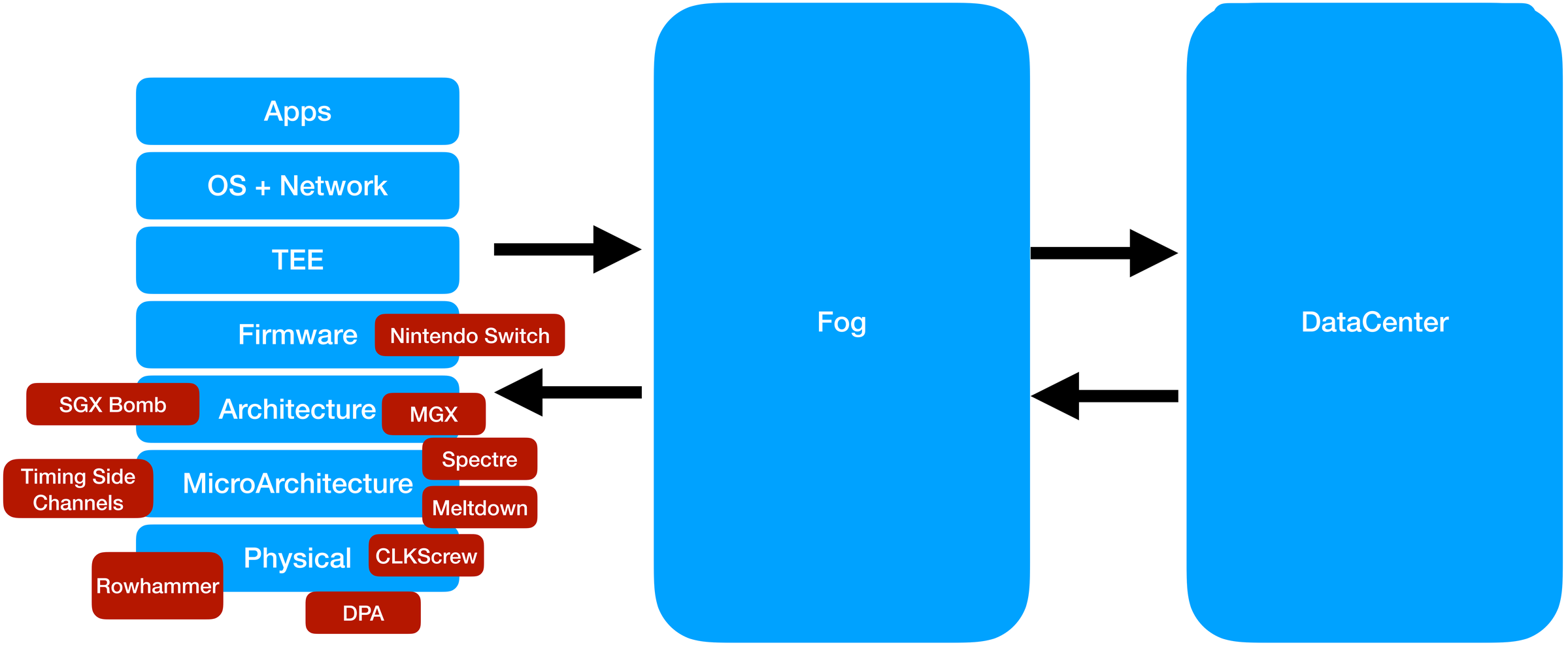
The IoT security problem



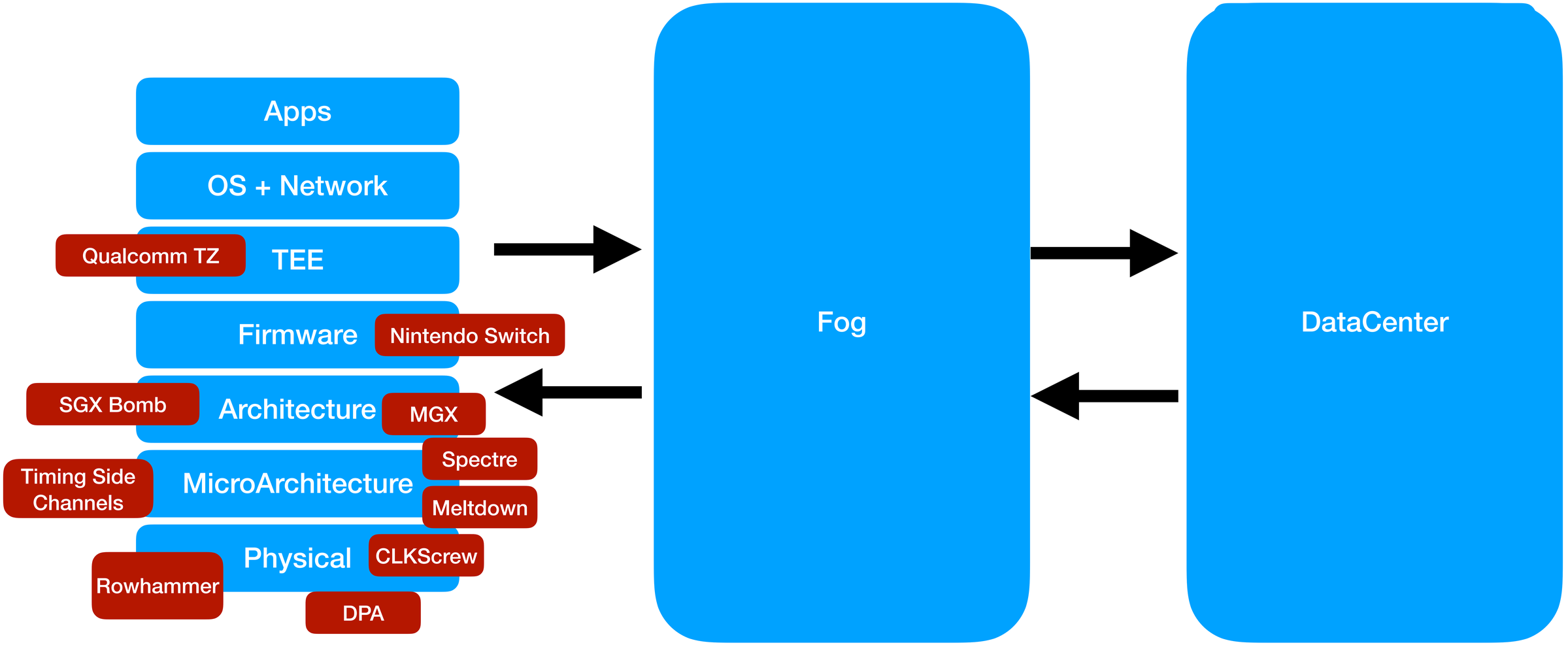
The IoT security problem



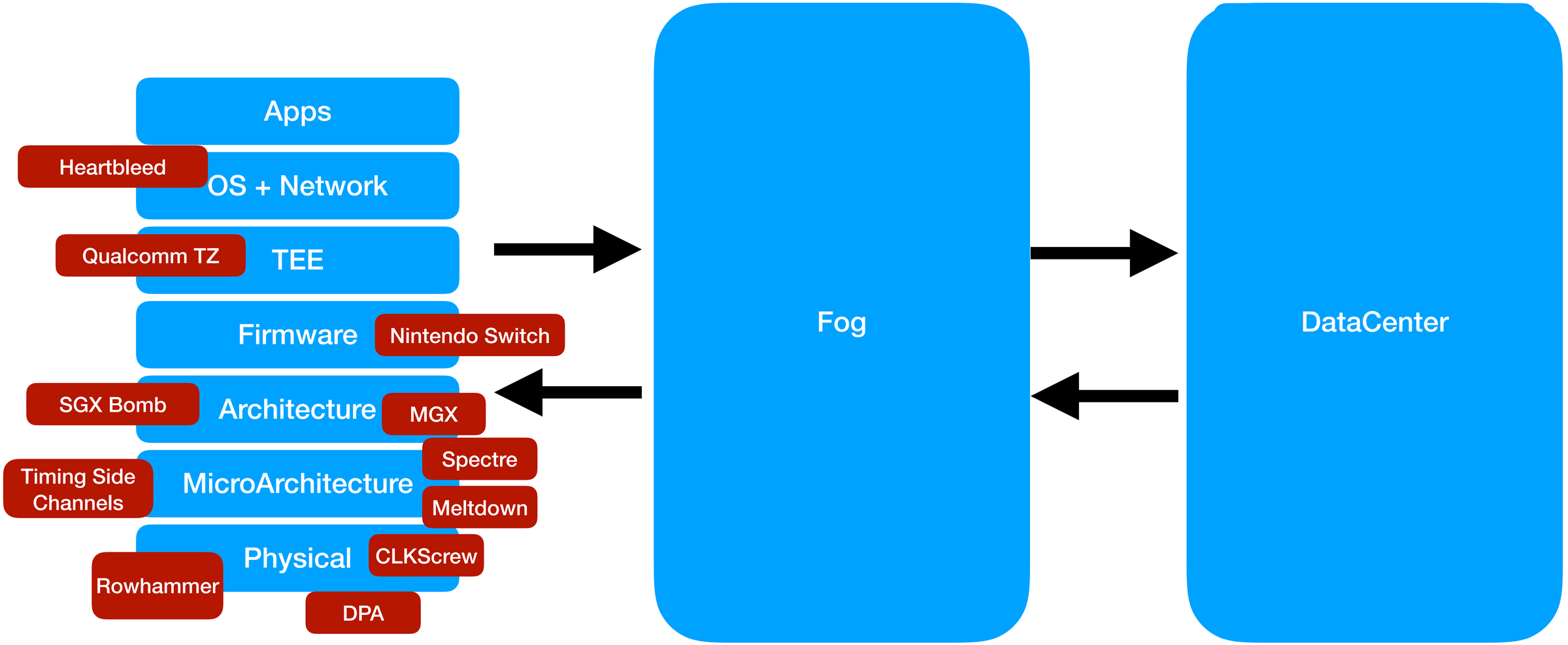
The IoT security problem



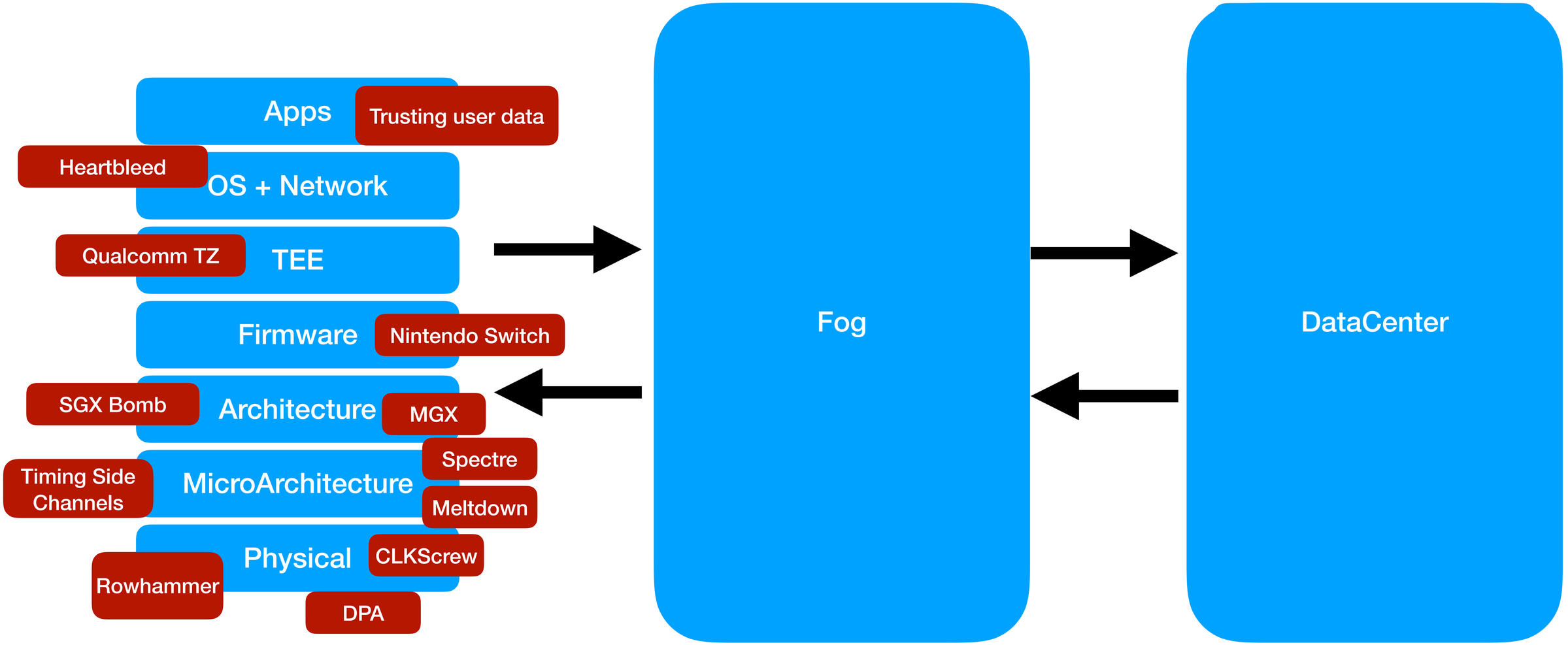
The IoT security problem



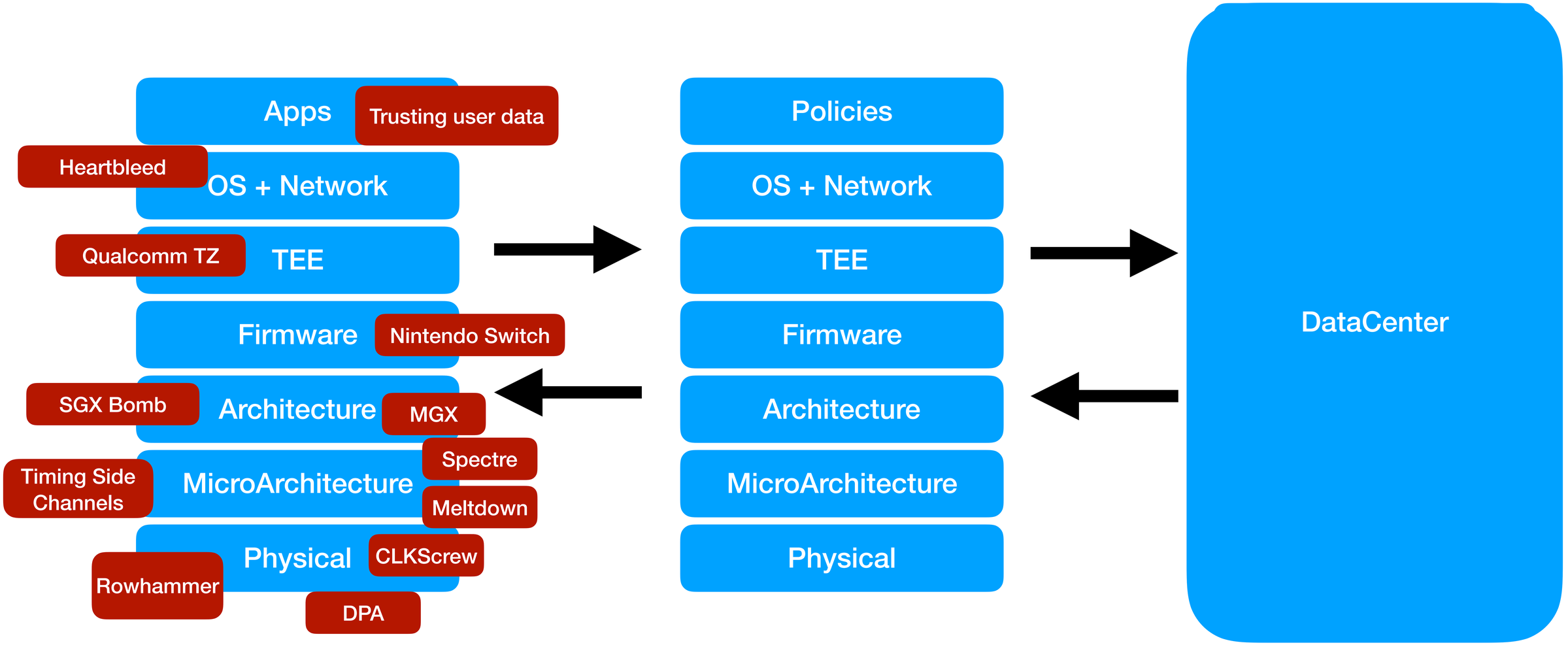
The IoT security problem



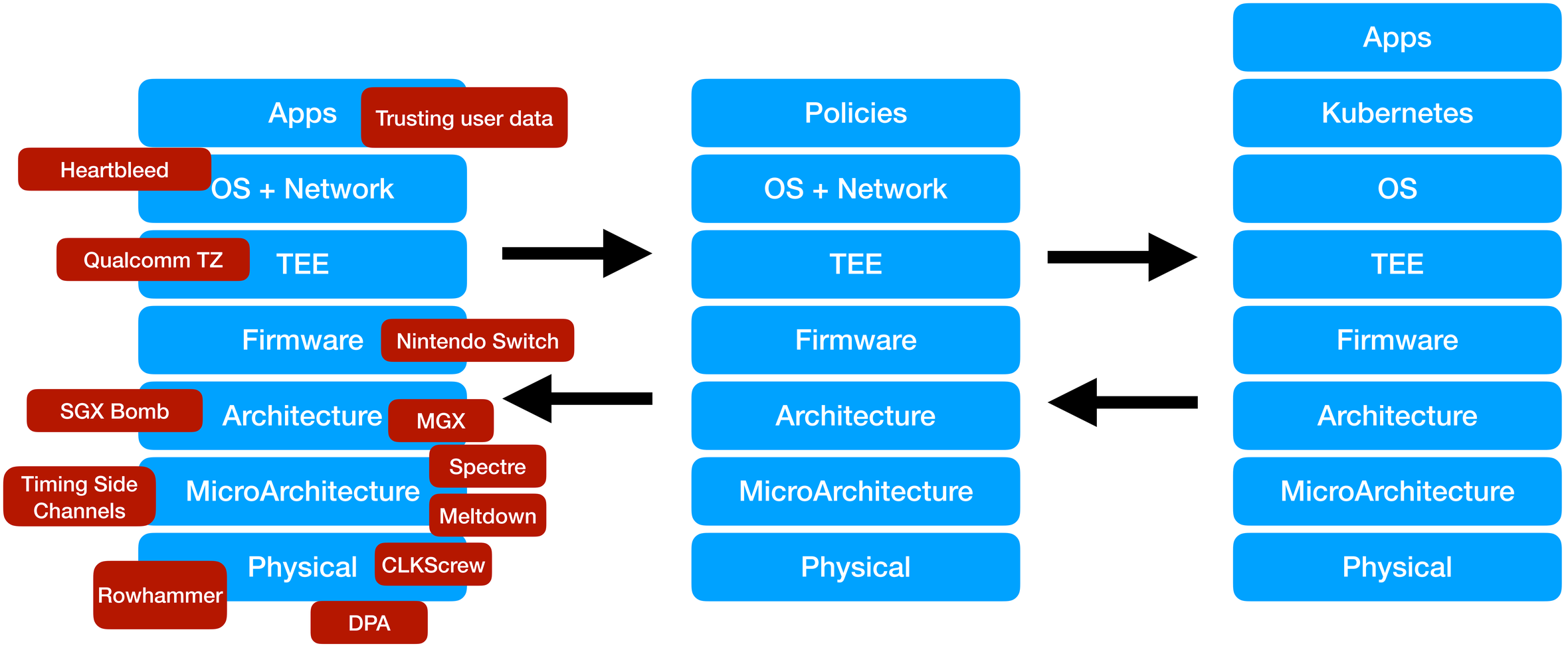
The IoT security problem



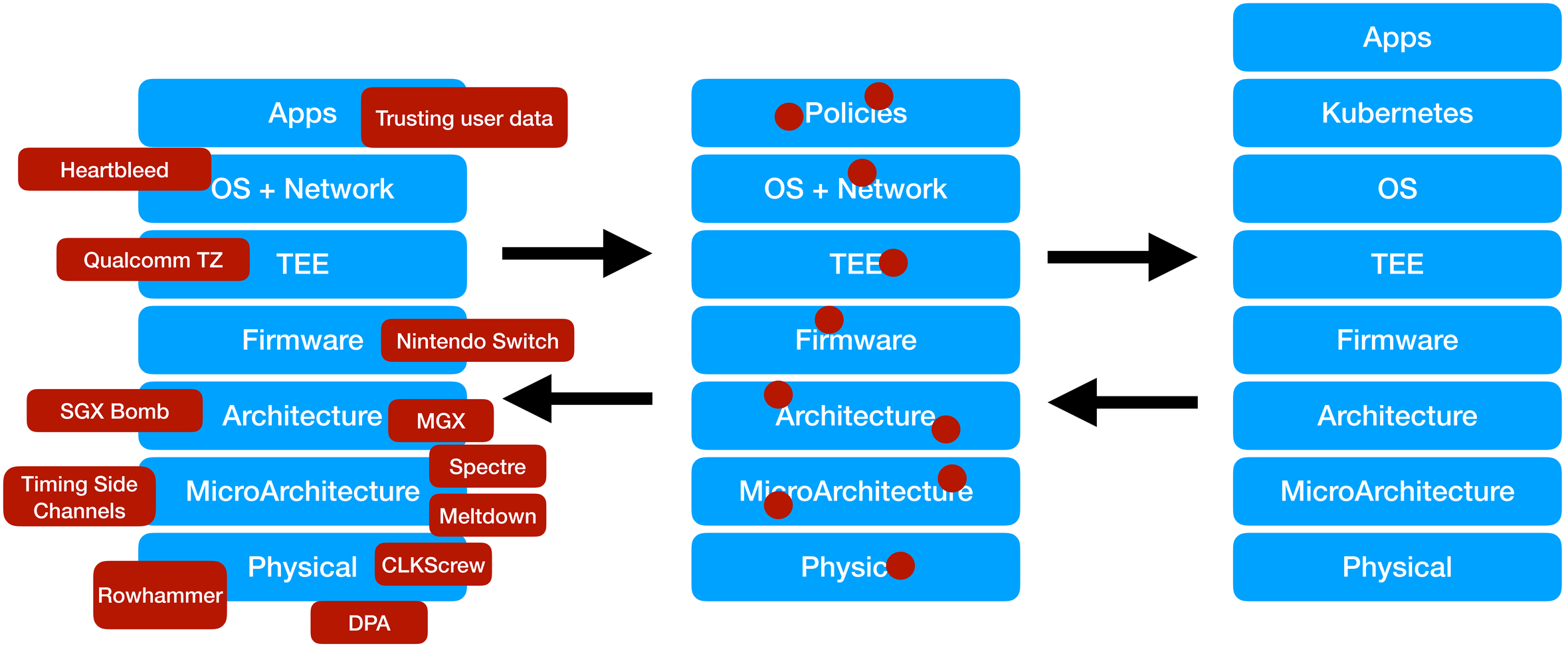
The IoT security problem



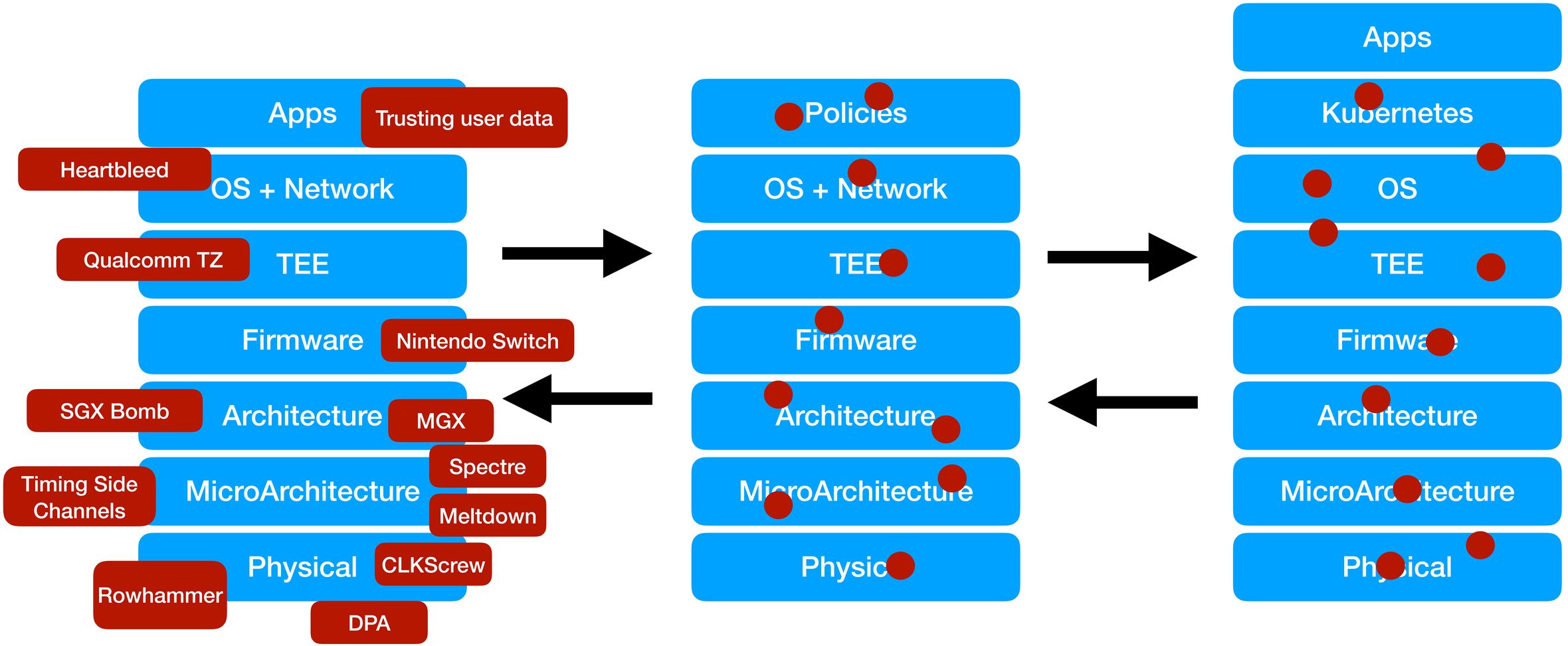
The IoT security problem



The IoT security problem



The IoT security problem



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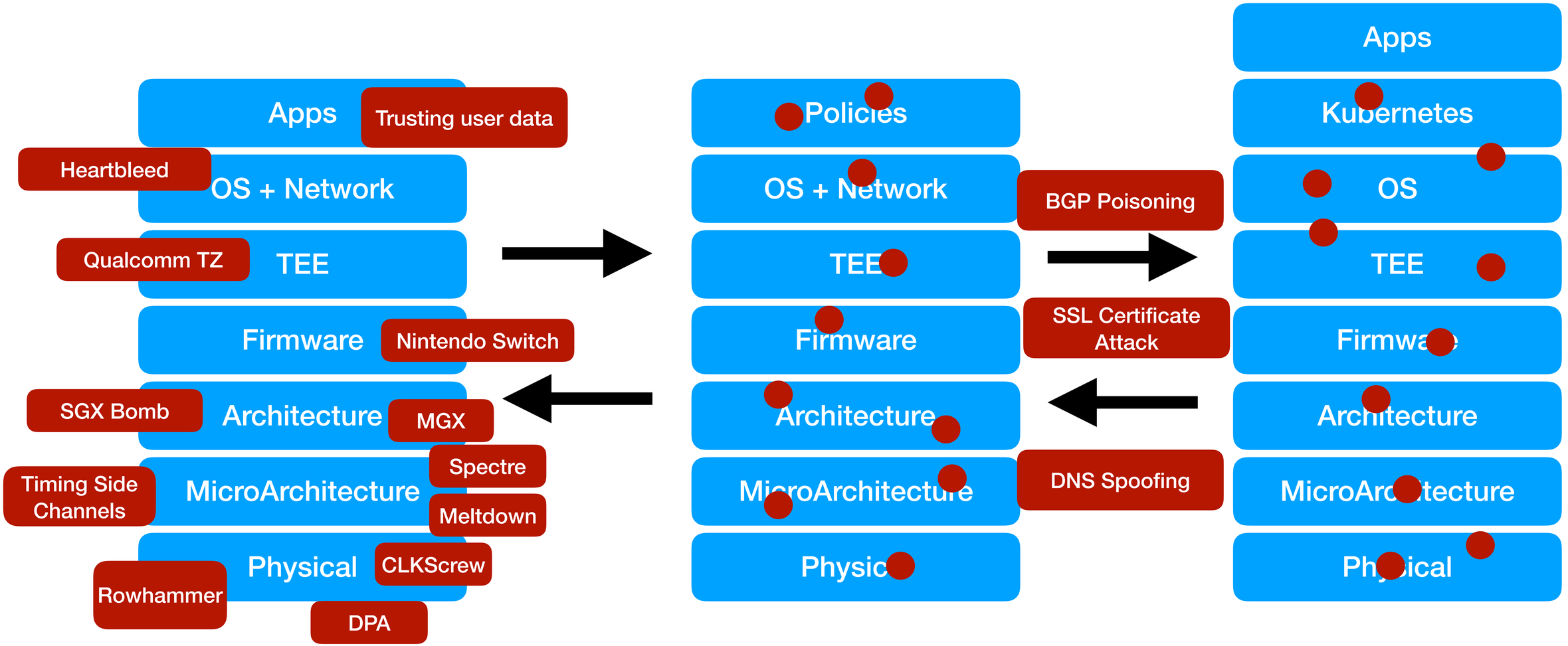


Reasoning about software and hardware

Programming

Exploit Detection

Formal Verification

Reverse Engineering

Bug Finding

Simulation

Automatic Test Generation

Fuzz Testing

Glitching

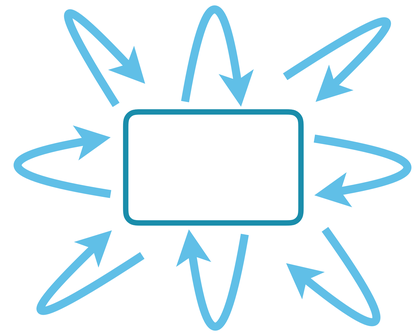
DPA

arm

Current status of ARM specifications

- Formal specifications of A, R and M-class processor classes exist
- Integrated into ARM’s official processor specifications
- Maintained by ARM’s architecture team
- Used by multiple teams within ARM
  - Formal validation of ARM processors using Bounded Model Checking
  - Development of test suites
  - Designing architecture extensions
  - …
- Publicly released in machine readable form

Overview



1. Reasoning about programs
2. ARM's formal processor specifications
   - Three experiences
   - Lessons learned
   - (Work in progress)
3. Conclusions

"Trustworthy Specifications of the ARM v8-A and v8-M architecture," FMCAD 2016
"End to End Verification of ARM processors with ISA Formal," CAV 2016
"Who guards the guards? Formal Validation of ARM v8-M Specifications," OOPSLA 2017
https://alastairreid.github.io/papers/

arm

“Trustworthy Specifications of the ARM v8-A and v8-M architecture,” FMCAD 2016

Creating trustworthy specifications

arm

Unstructured English Prose (A-class spec)

Concurrent modification and execution of instructions

The ARMv8 architecture limits the set of instructions that can be executed by one thread of execution as they are being modified by another thread of execution without requiring explicit synchronization.

Concurrent modification and execution of instructions can lead to the resulting instruction performing any behavior that can be achieved by executing any sequence of instructions that can be executed from the same Exception level, except where each of the instruction before modification and the instruction after modification is one of a `B`, `BL`, `BRK`, `HVC`, `ISB`, `NOP`, `SMC`, or `SVC` instruction.

For the `B`, `BL`, `BRK`, `HVC`, `ISB`, `NOP`, `SMC`, and `SVC` instructions the architecture guarantees that, after modification of the instruction, behavior is consistent with execution of either:

- The instruction originally fetched.
- A fetch of the modified instruction.

If one thread of execution changes a conditional branch instruction, such as `B` or `BL`, to another conditional instruction and the change affects both the condition field and the branch target, execution of the changed instruction by another thread of execution before the change is synchronized can lead to either:

- The old condition being associated with the new target address.
- The new condition being associated with the old target address.

These possibilities apply regardless of whether the condition, either before or after the change to the branch instruction, is the *always* condition.

Semi-structured English prose (M-class spec)

R_{JRJC}

Exit from lockup is by any of the following:

- A Cold reset.
- A Warm reset.
- Entry to Debug state.
- Preemption by a higher priority exception.

R_{VGNW}

Entry to lockup from an exception causes:

- Any Fault Status Registers associated with the exception to be updated.
- No update to the exception state, pending or active.
- The PC to be set to `0xEFFFFFFE`.
- EPSR.IT to be become UNKNOWN.

In addition, HFSR.FORCED is not set to 1.

arm

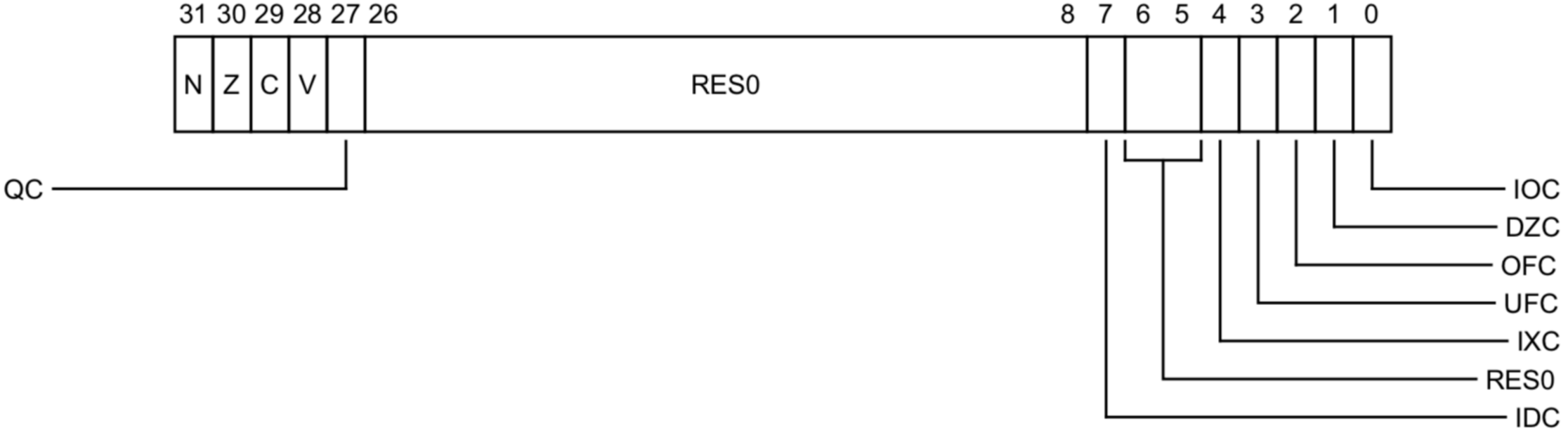
Tables - semistructured, not machine readable

Table B2-1 Encoding of the DMB and DSB <option> parameter

Accesses		Shareability domain			
Before the barrier	**After the barrier**	**Full system**	**Outer Shareable**	**Inner Shareable**	**Non-shareable**
Reads and writes	Reads and writes	SY	OSH	ISH	NSH
Writes	Writes	ST	OSHST	ISHST	NSHST
Reads	Reads and writes	LD	OSHLD	ISHLD	NSHLD

arm

Registers - structured, machine-readable



N, bit [31]

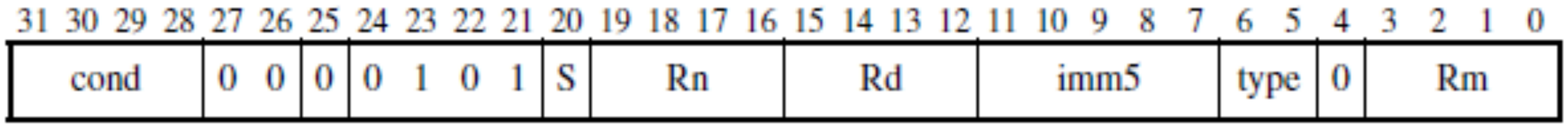
Negative condition flag for AArch32 floating-point comparison operations. AArch64 floating-point comparisons set the PSTATE.N flag instead.

Z, bit [30]

Zero condition flag for AArch32 floating-point comparison operations. AArch64 floating-point comparisons set the PSTATE.Z flag instead.

Pseudocode

```
ADC{S}<c> <Rd>,<Rn>,<Rm>{,<shift>}
```



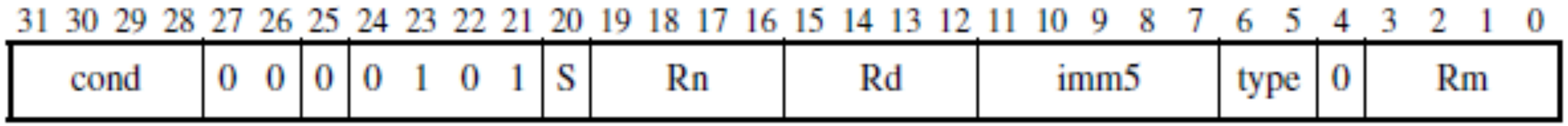
31 30 29 28	27 26	25	24 23 22 21	20	19 18 17 16	15 14 13 12	11 10 9 8 7	6 5	4	3 2 1 0
cond	0 0	0	0 1 0 1	S	Rn	Rd	imm5	type	0	Rm

```
if Rd == '1111' && S == '1' then SEE SUBS PC, LR and related instructions;
d = UInt(Rd);  n = UInt(Rn);  m = UInt(Rm);  setflags = (S == '1');
(shift_t, shift_n) = DecodeImmShift(type, imm5);

if ConditionPassed() then
    EncodingSpecificOperations();
    shifted = Shift(R[m], shift_t, shift_n, APSR.C);
    (result, carry, overflow) = AddWithCarry(R[n], shifted, APSR.C)
    if d == 15 then          // Can only occur for ARM encoding
        ALUWritePC(result);  // setflags is always FALSE here
    else
        R[d] = result;
        if setflags then
            APSR.N = result<31>;
            APSR.Z = IsZeroBit(result);
            APSR.C = carry;
            APSR.V = overflow;
```

Pseudocode

```
ADC{S}<c> <Rd>,<Rn>,<Rm>{,<shift>}
```



31 30 29 28	27 26	25	24 23 22 21	20	19 18 17 16	15 14 13 12	11 10 9 8 7	6 5	4	3 2 1 0
cond	0 0	0	0 1 0 1	S	Rn	Rd	imm5	type	0	Rm

```
if Rd == '1111' && S == '1' then SEE SUBS PC, LR and related instructions;
d = UInt(Rd);  n = UInt(Rn);  m = UInt(Rm);  setflags = (S == '1');
(shift_t, shift_n) = DecodeImmShift(type, imm5);

if ConditionPassed() then
    EncodingSpecificOperations();
    shifted = Shift(R[m], shift_t, shift_n, APSR.C);
    (result, carry, overflow) = AddWithCarry(R[n], shifted, APSR.C)
    if d == 15 then          // Can only occur for ARM encoding
        ALUWritePC(result);  // setflags is always FALSE here
    else
        R[d] = result;
        if setflags then
            APSR.N = result<31>;
            APSR.Z = IsZeroBit(result);
            APSR.C = carry;
            APSR.V = overflow;
```

- Type Inference
- Unbounded Integers
- Enumerations
- Bit Vectors
- Indentation-based Syntax
- Dependent Types
- Imperative
- Exceptions

arm

Status at the start

- No tools (parser, type checker)
- Incomplete (around 15% missing)
  - “Specify by comment”
  - Many trivial errors (that confuse tools but not humans)
- Unexecuted, untested
- Senior architects believed that an executable spec was
  - Impossible
  - Not useful
  - Less readable
  - Less correct

Architectural Conformance Suite

Processor architectural compliance sign-off

Large

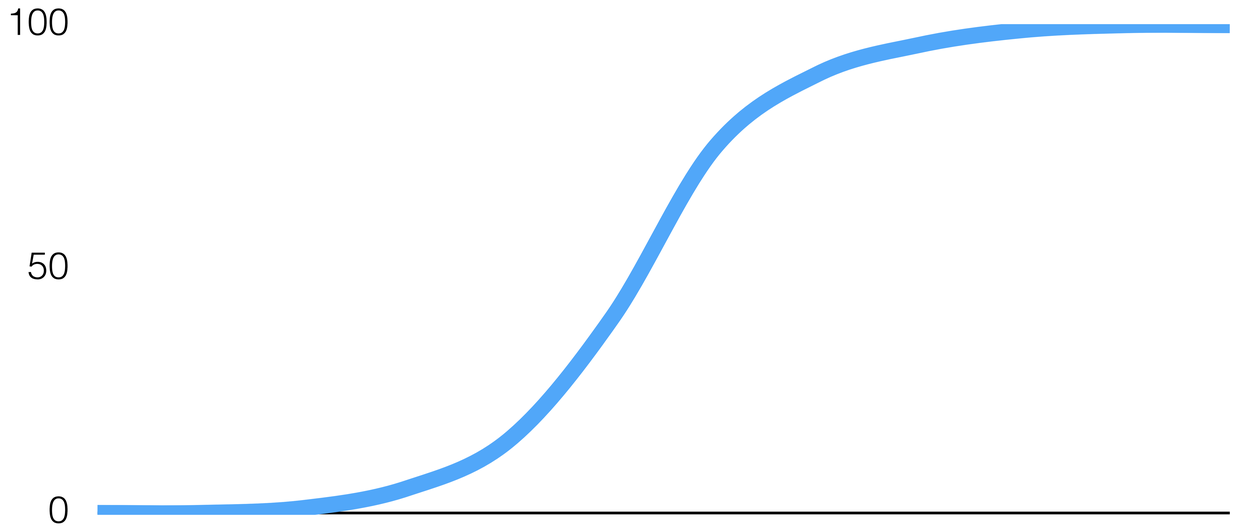
- v8-A 32,000 test programs, billions of instructions
- v8-M 3,500 test programs, > 250 million instructions

Thorough

- Tests dark corners of specification

arm

Progress in testing Arm specification



- Does not parse, does not typecheck
- Can’t get out of reset
- Can’t execute first instruction
- Can’t execute first 100 instructions
- …
- Passes 90% of tests
- Passes 99% of tests
- …

arm

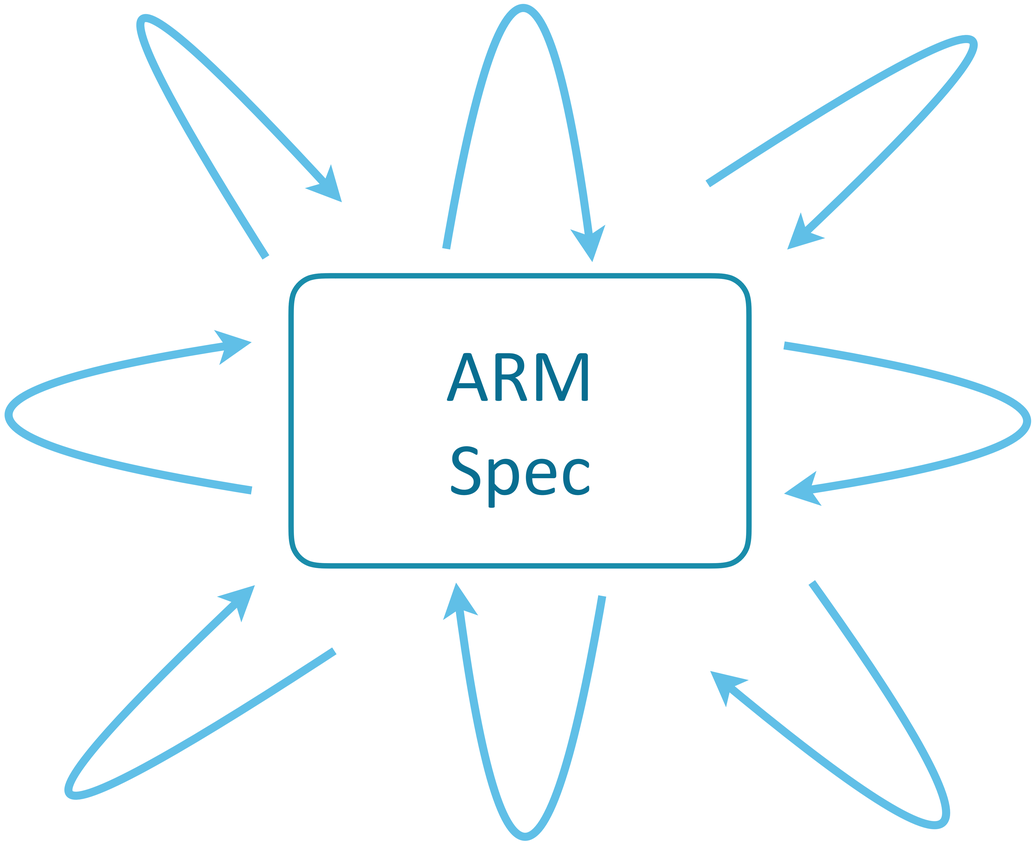
Measuring architecture coverage of tests

Untested: op1*op2 == -3.0, FPCR.RND=-Inf


```
bits(N) FPRSqrtStepFused(bits(N) op1, bits(N) op2)
    assert N IN {32, 64};
    bits(N) result;
    op1 = FPNeg(op1);    // per FMSUB/FMLS
    (type1,sign1,value1) = FPUnpack(op1, FPCR);
    (type2,sign2,value2) = FPUnpack(op2, FPCR);
    (done,result) = FPProcessNaNs(type1, type2, op1, op2, FPCR);
    if !done then
        inf1 = (type1 == FPType_Infinity);
        inf2 = (type2 == FPType_Infinity);
        zero1 = (type1 == FPType_Zero);
        zero2 = (type2 == FPType_Zero);
        if (inf1 && zero2) || (zero1 && inf2) then
            result = FPOnePointFive('0');
        elsif inf1 || inf2 then
            result = FPInfinity(sign1 EOR sign2, N);
        else
            // Fully fused multiply-add and halve
            result_value = (3.0 + (value1 * value2)) / 2.0;
            if result_value == 0.0 then
                // Sign of exact zero result depends on rounding mode
                sign = if FPCRRounding() == FPRounding_NEGINF then '1' else '0';
                result = FPZero(sign, N);
            else
                result = FPRound(result_value, FPCRRounding());
    return result;
```


arm

Creating a Virtuous Cycle



arm

Lessons learned about engineering a specification

Specifications contain bugs

Huge value in being able to run existing test suites

- Need to balance against benefits of non-executable specs

Find ways to provide direct benefit to other users of spec

- They will do some of the testing/debugging for you
- They will support getting your changes/spec adopted as master spec
- Creates Virtuous Cycle

“End to End Verification of ARM processors with ISA Formal,” CAV 2016

“Who guards the guards? Formal Validation of ARM v8-M Specifications” OOPSLA 2017

Formal validation of processors and of specifications

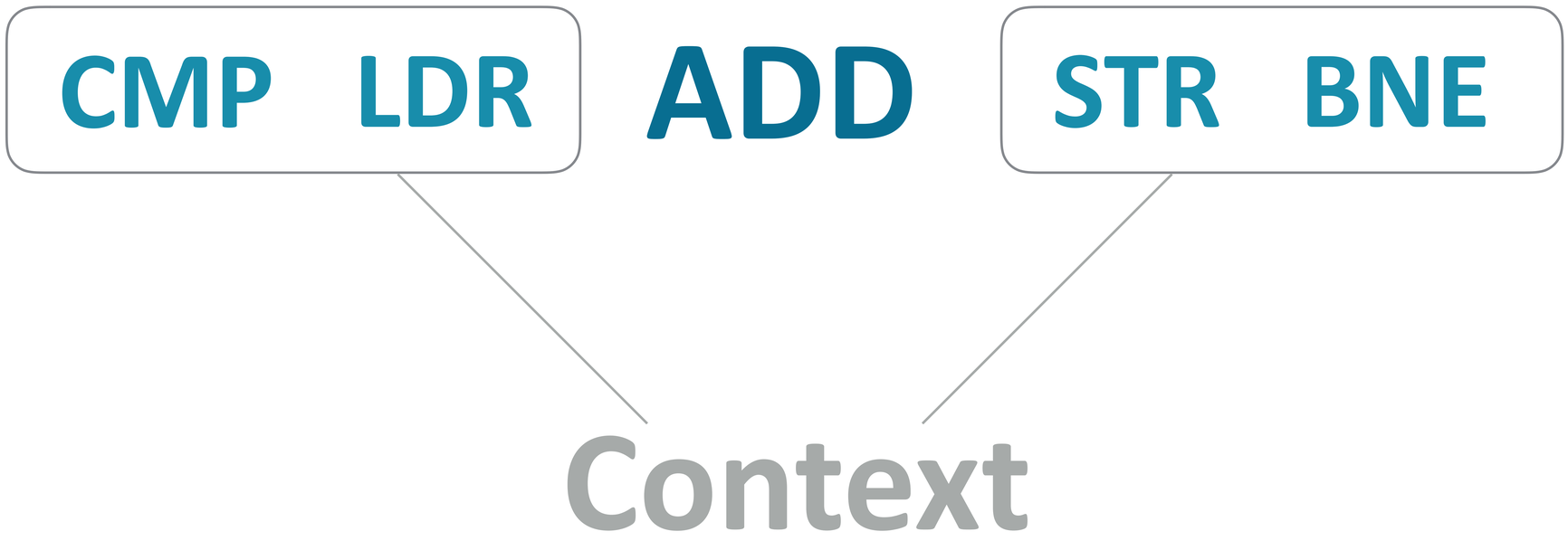
arm

Checking an instruction

ADD

arm

Checking an instruction



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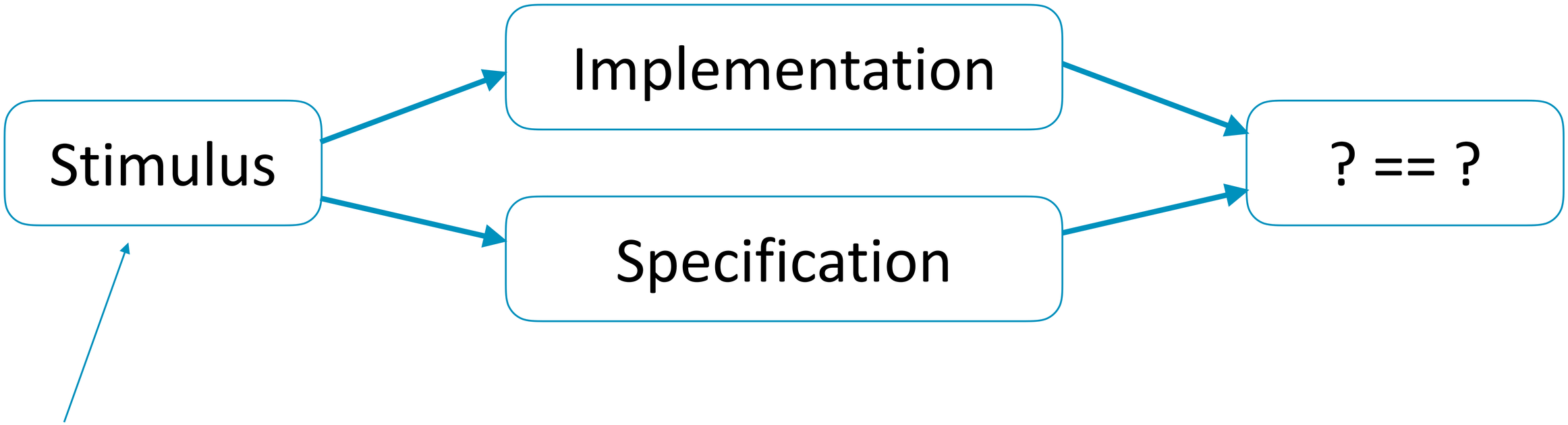
Formal framework (deterministic specs)



Bounded model checker

arm

Arm CPUs verified with ISA-Formal

A-class	R-class	M-class
Cortex-A53	Cortex-R52	Cortex-M4
Cortex-A32	Next generation	Cortex-M7
Cortex-A35		Cortex-M33
Cortex-A55		Next generation
Next generation		

Cambridge Projects

Rolling out globally to other design centres

Sophia, France - Cortex-A75 (partial)

Austin, USA - TBA

Chandler, USA - TBA

arm

Lessons Learned from validating processors

Very effective way to find bugs in implementations

Formally validating implementation is effective at finding bugs in spec

- Try to find most of the bugs in your spec before you start

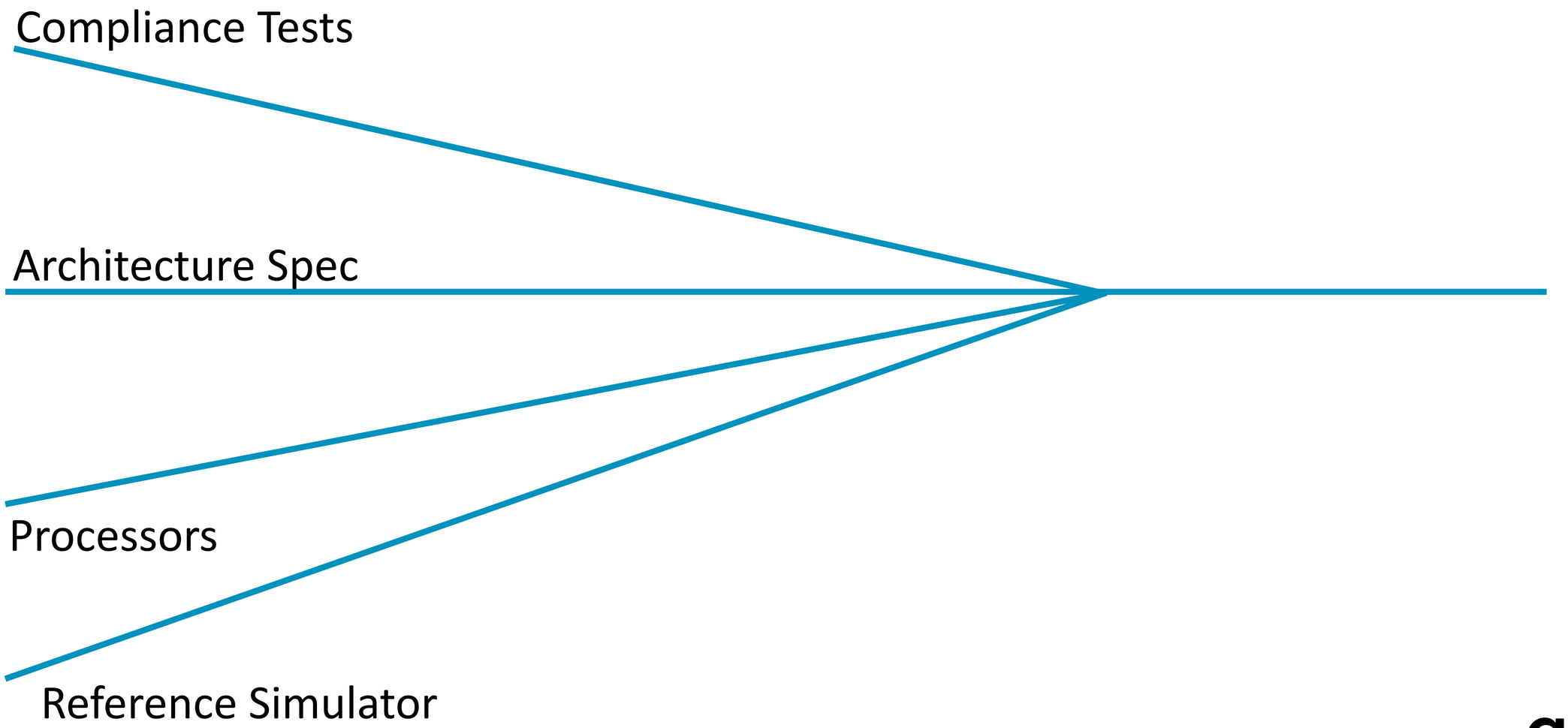
Huge value in being able to use spec to validate implementations

- Helps get formal specification adopted as part of official spec

Formal validation of specifications

arm

One Specification to rule them all?



arm

Rule JRJC

Exit from lockup is by any of the following:

- A Cold reset.
- A Warm reset.
- Entry to Debug state.
- Preemption by a higher priority processor exception.

Rule R

State Change X is by any of the following:

- Event A
- Event B
- State Change C
- Event D

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Rule R

State Change X is by any of the following:

- Event A
- Event B
- State Change C
- Event D

Rule R: $X \rightarrow A \vee B \vee C \vee D$

arm

State Change	Exit from lockup	Fell(LockedUp)
Event	A Cold reset	Called(TakeColdReset)
Event	A Warm reset	Called(TakeReset)
State Change	Entry to Debug state	Rose(Halted)
Event	Preemption by a higher priority processor exception	Called(ExceptionEntry)

arm

“Eyeball Closeness”

Rule JRJC

Exit from lockup is by any of the following:

- A Cold reset.
- A Warm reset.
- Entry to Debug state.
- Preemption by a higher priority processor exception.

$$\begin{aligned} Fell(LockedUp) \rightarrow\ & Called(TakeColdReset) \\ \vee\ & Called(TakeReset) \\ \vee\ & Rose(Halted) \\ \vee\ & Called(ExceptionEntry) \end{aligned}$$

Rule VGNW

Entry to lockup from an exception causes

- Any Fault Status Registers associated with the exception to be updated.

Out of date
- No update to the exception state, pending or active.

Misleading
- The PC to be set to 0xEFFFFFFE.

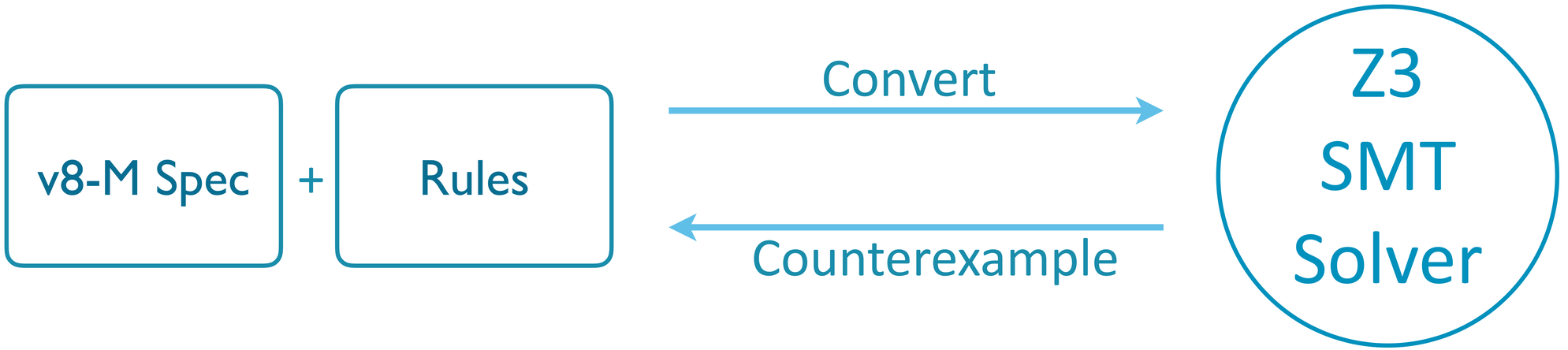
Untestable
- EPSR.IT to become UNKNOWN.

Ambiguous

In addition, HFSR.FORCED is not set to 1.

~10,000 lines

~1,000,000 lines



arm

Lessons Learned from validating specifications

Redundancy essential for detecting errors

- Detected subtle bugs in security, exceptions, debug, …

- Found bugs in English prose

Need set of ‘orthogonal’ properties

- Invariants, Security properties, Reachability properties, etc.

Eyeball closeness

Needed to translate specification to another language to let us use other tools

Work in progress:
Security of architecture specifications

arm

Validating security of processor architectures

Scope

- Compositional Attacks

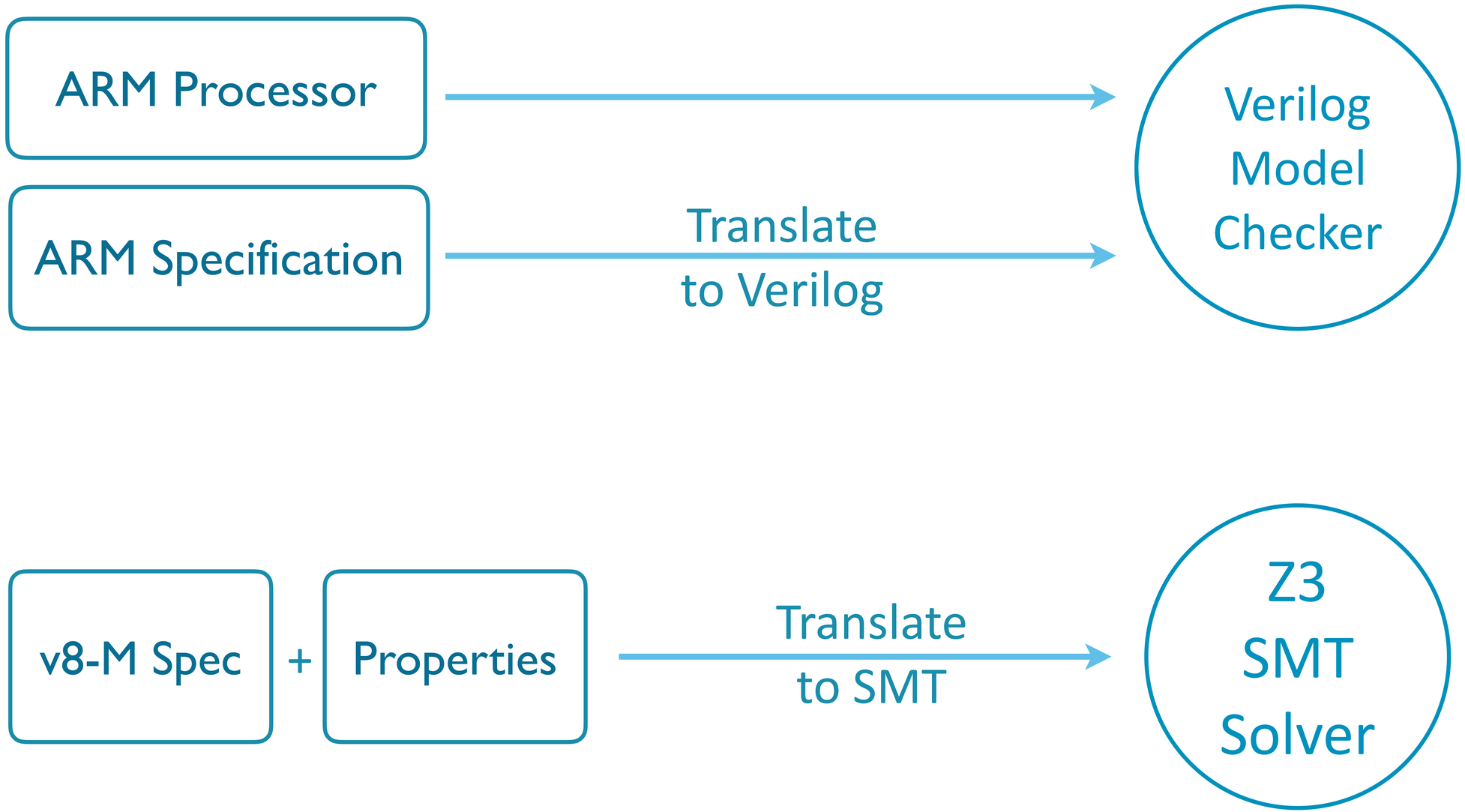
- Hardware-based Security Enforcement

- Confidentiality, Integrity, Availability (and more?)

Challenges

- Cyclic dependencies between HSEs

- Microarchitectural storage/timing channels



arm

Engineering Formal Specifications of Real World Artifacts

Plan for adoption into official specs

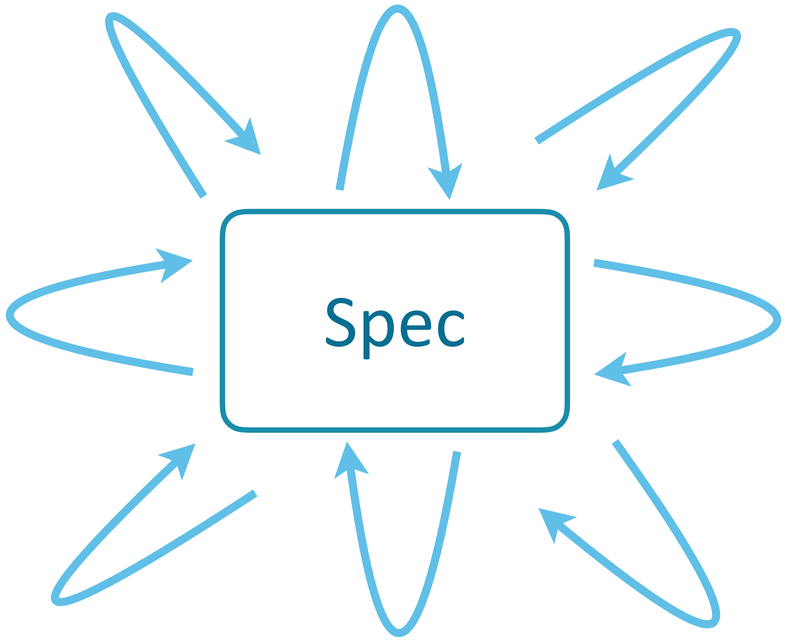
Apply standard engineering practices

- Test, review, CI, …
- Understand approximations and limitations

Build a virtuous cycle

- Look for early adopters
- What is “killer app” of your spec?
- Ensure specifications have many uses

  (Don’t write spec in Coq / HOL / ACL2 / …)



arm

Public release of machine readable Arm specification

Enable formal verification of software and tools

Releases: v8.2 (4/2017), v8.3 (10/2017), v8.4 (6/2018), v8.5 (9/2018)

Working with Cambridge University REMS group to convert to SAIL

Backends for HOL, OCaml, Memory model, (hopefully Coq too)

Specification: https://developer.arm.com/products/architecture/a-profile/exploration-tools

Tools: https://github.com/alastairreid/mra_tools

(See also: https://github.com/herd/herdtools7/blob/master/herd/libdir/aarch64.cat)

Talk to me about how I can help you use it

Thank You!
Danke!
Merci!
谢谢!
ありがとう!
Gracias!
Kiitos!

@alastair_d_reid

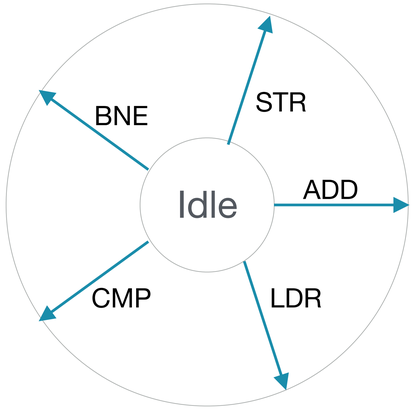
arm

“Trustworthy Specifications of the ARM v8-A and v8-M architecture,” FMCAD 2016

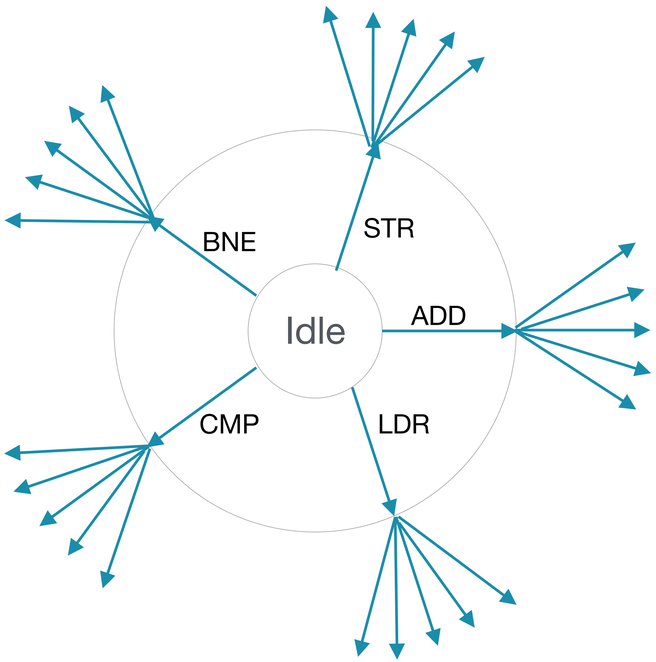
“End to End Verification of ARM processors with ISA Formal,” CAV 2016

“Who guards the guards? Formal Validation of ARM v8-M Specifications,” OOPSLA 2017

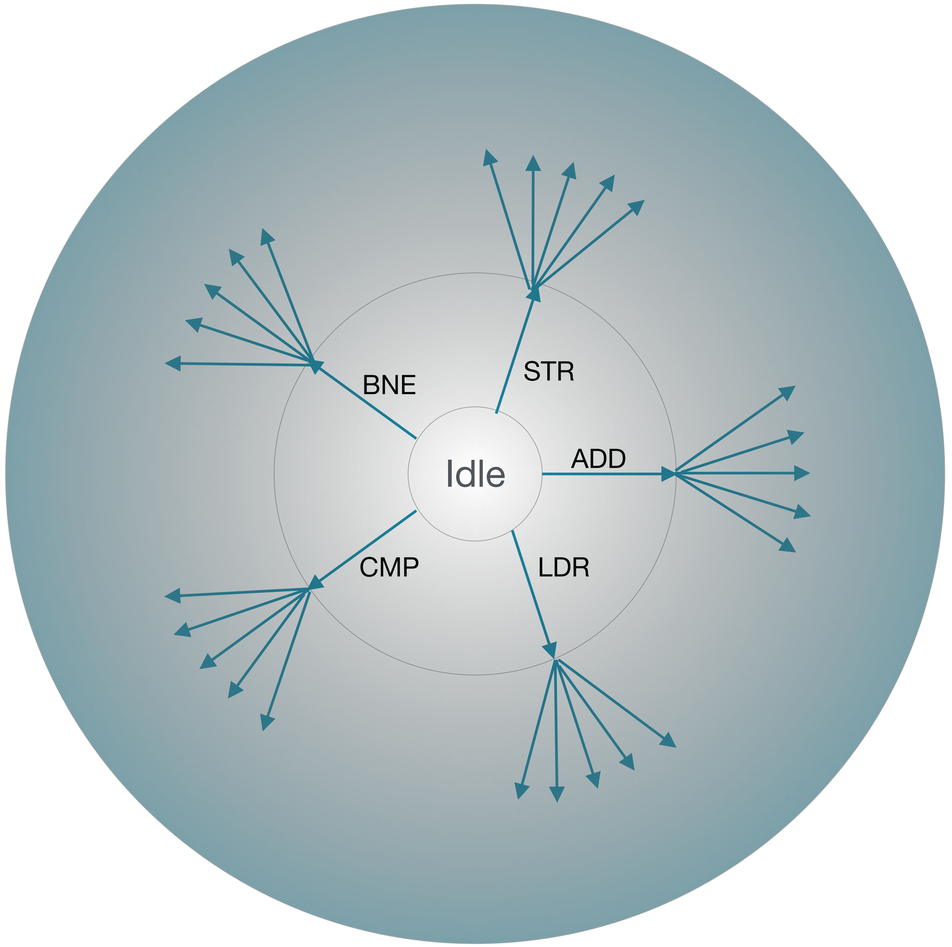
Formal verification is breadth first



Formal verification is breadth first



Formal verification is breadth first



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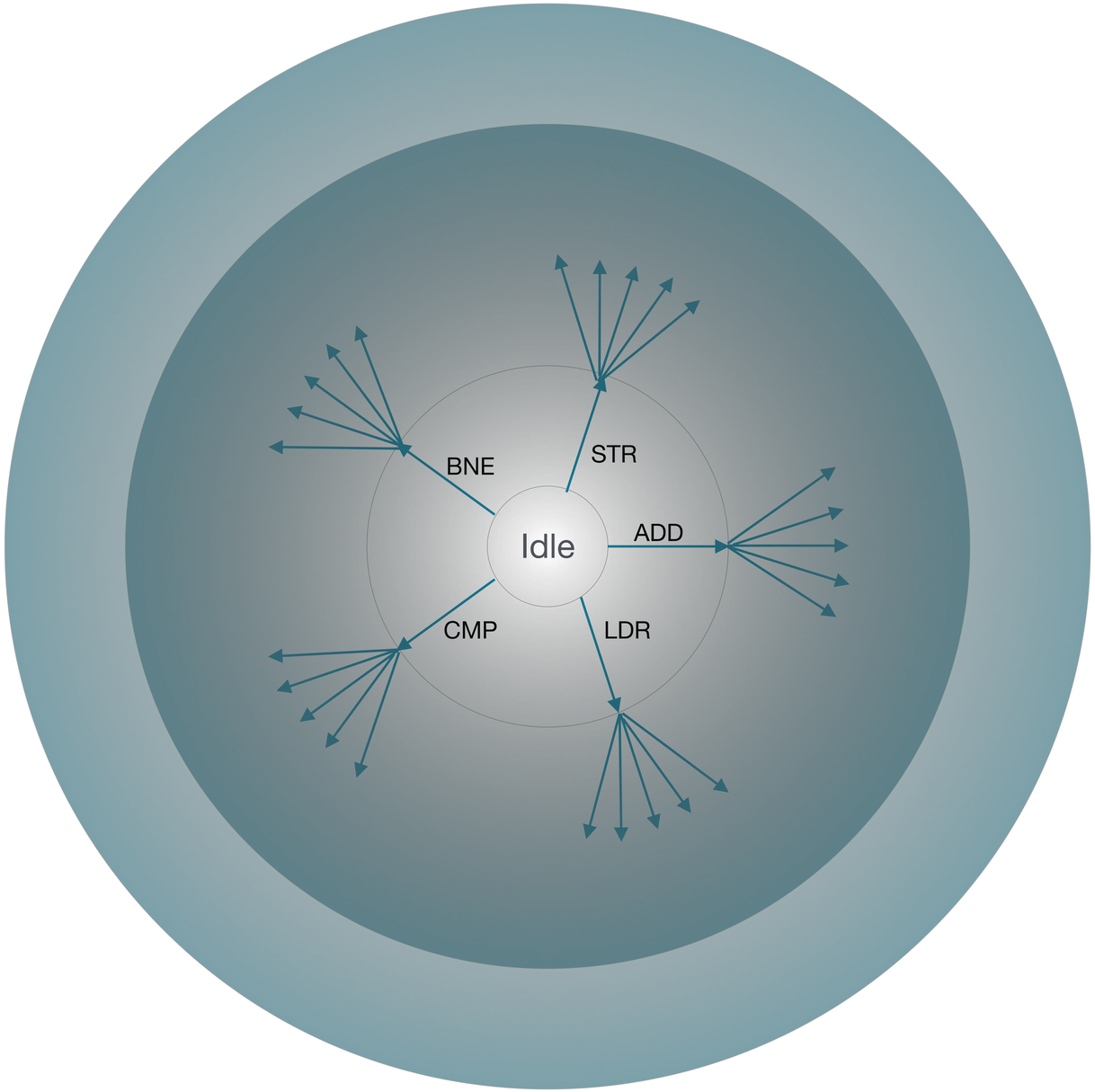

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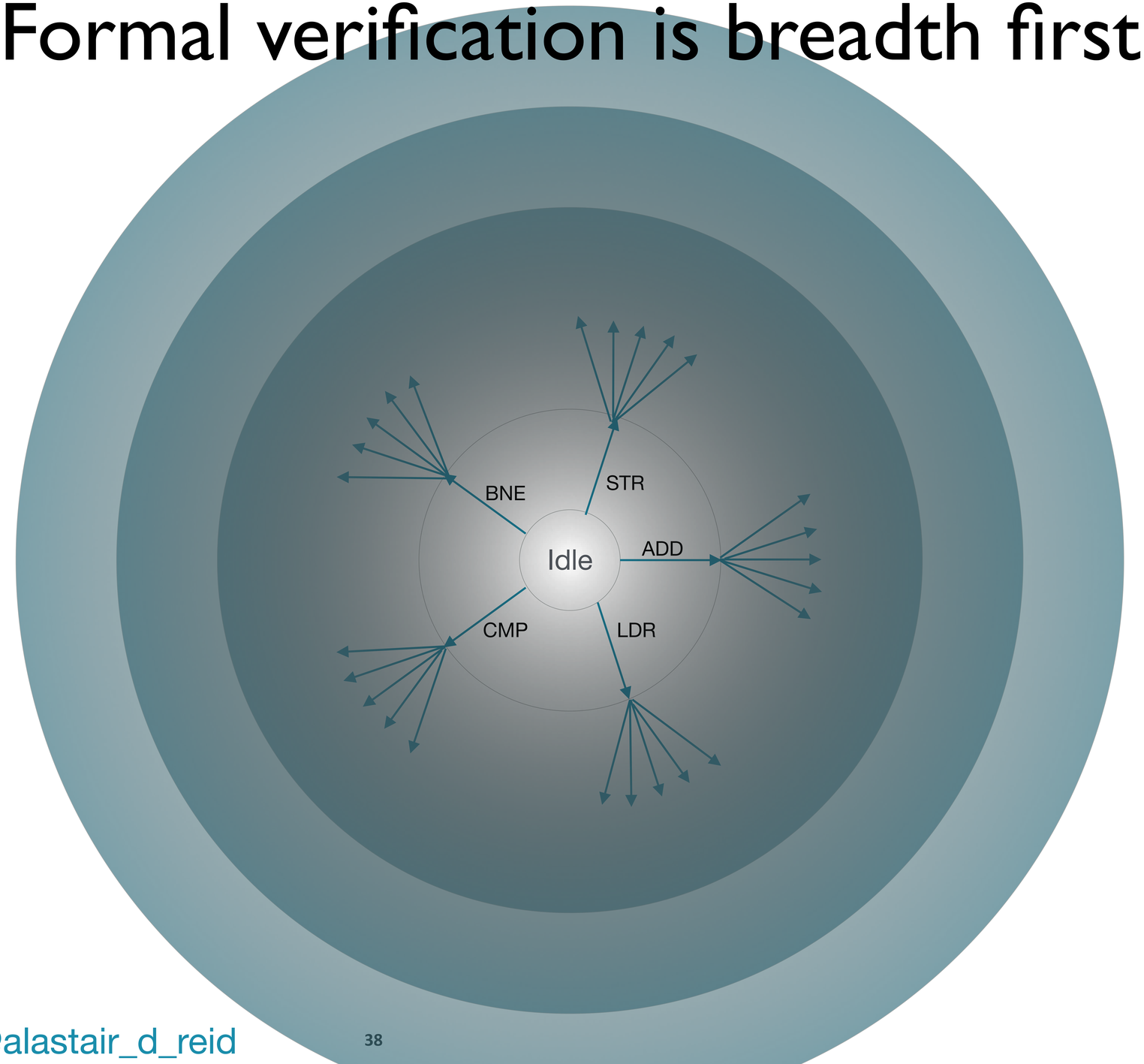

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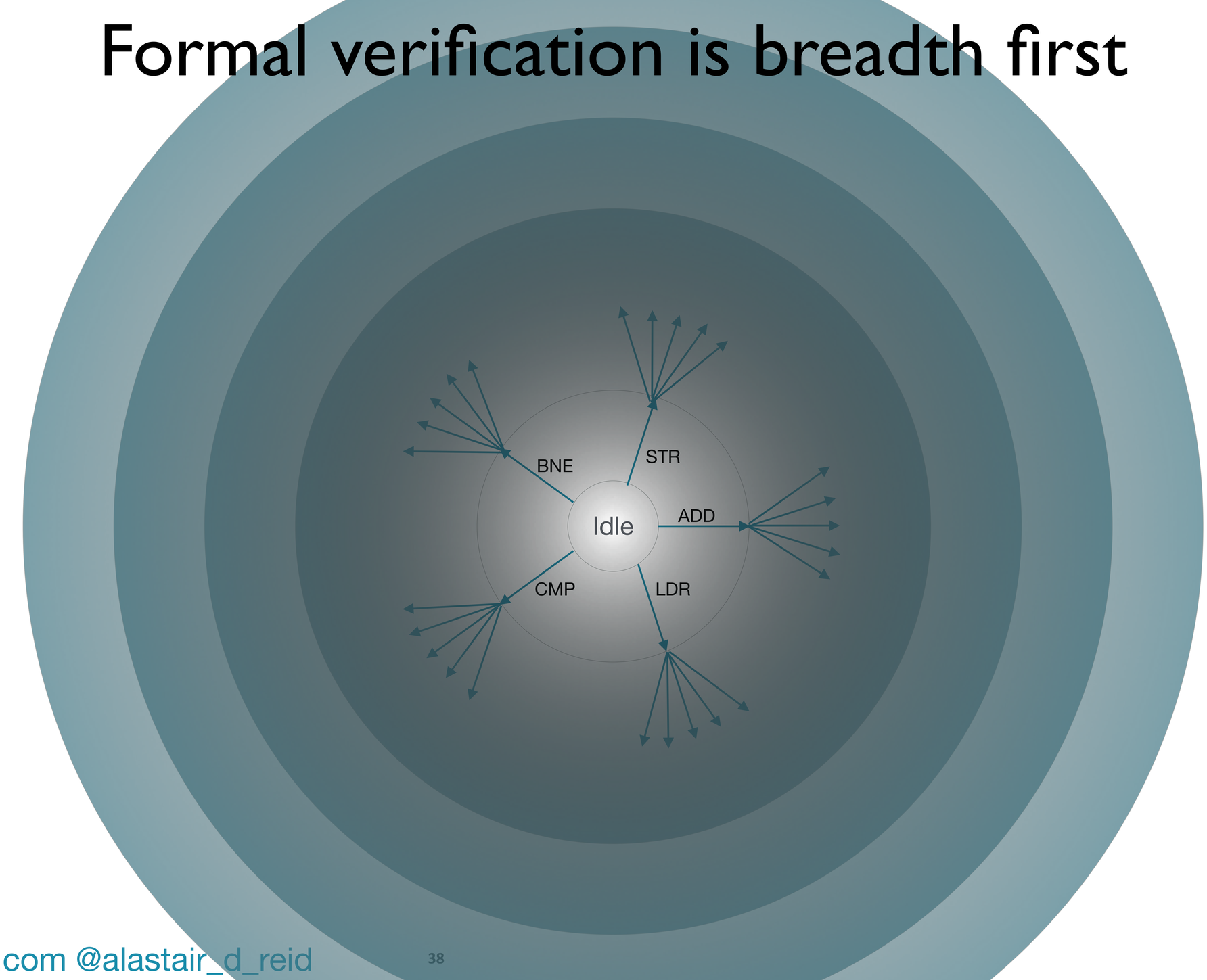
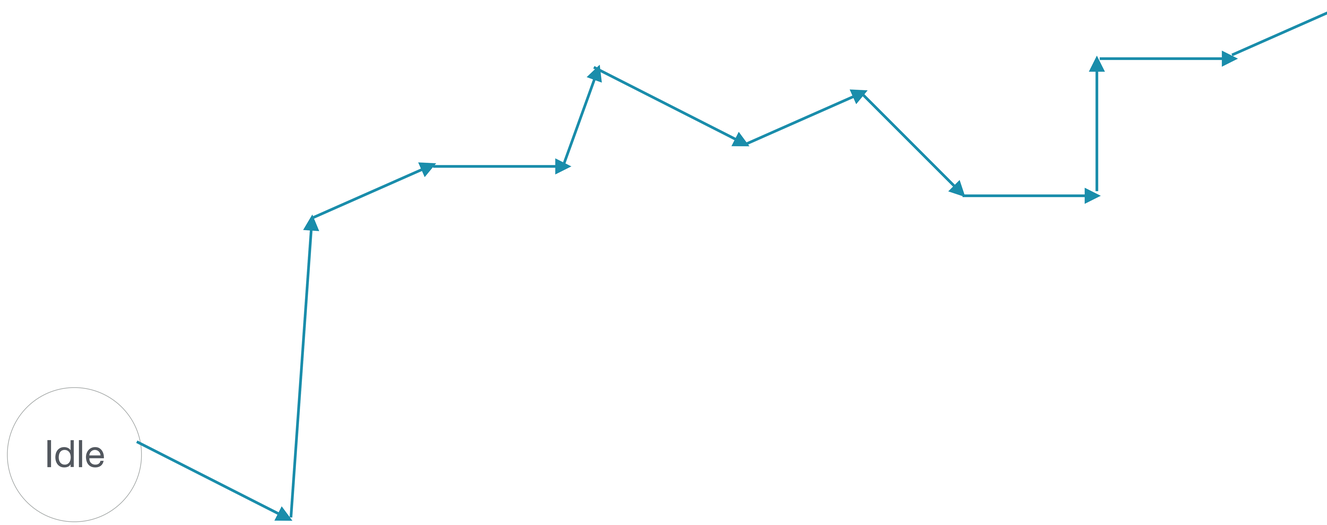


Testing is depth-first

Testing is depth-first



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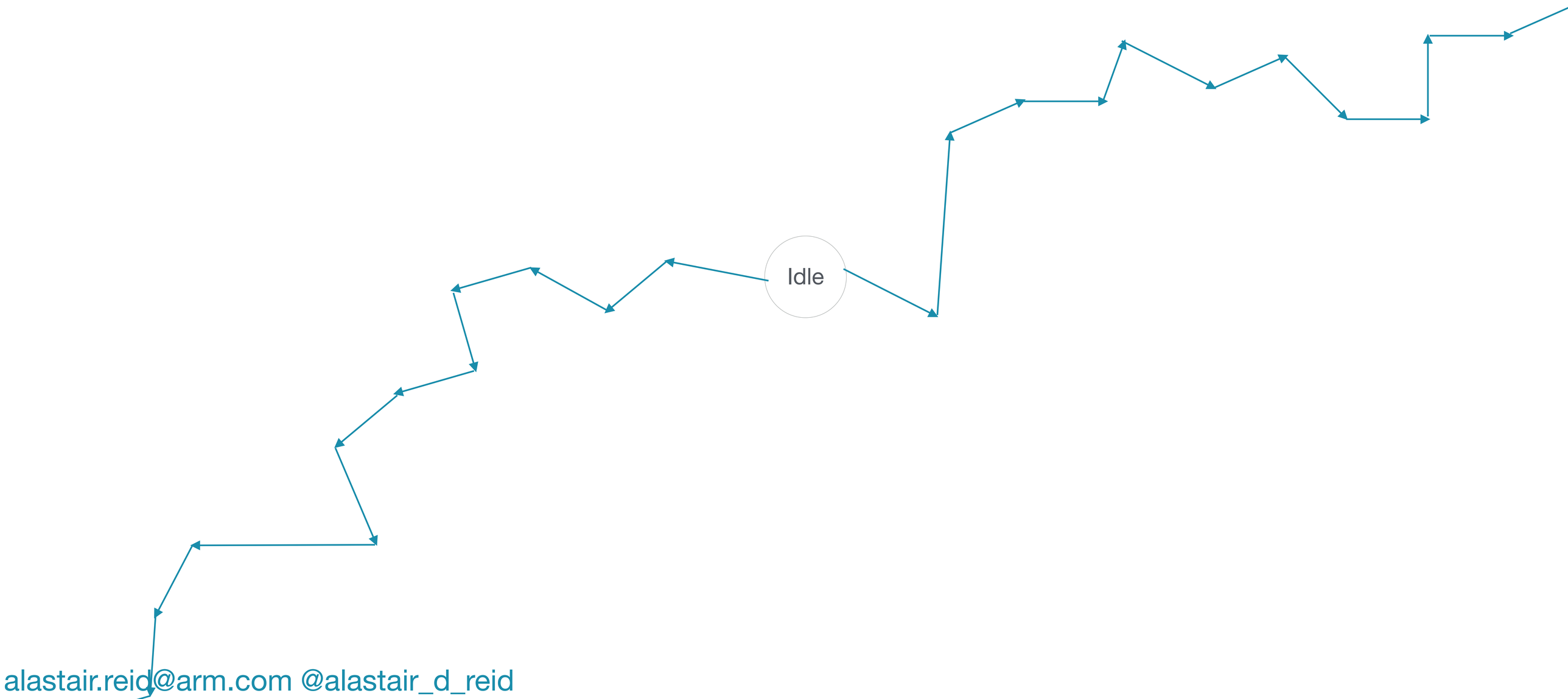

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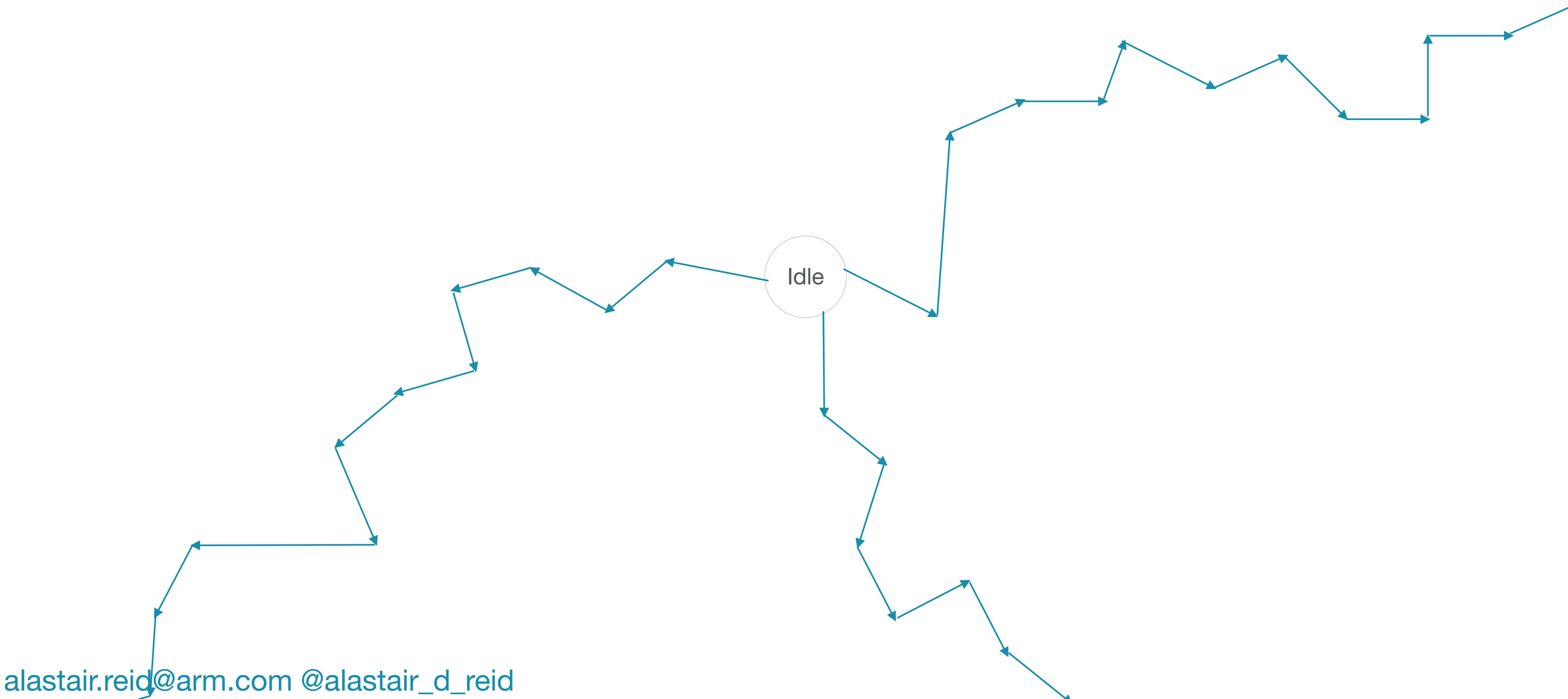

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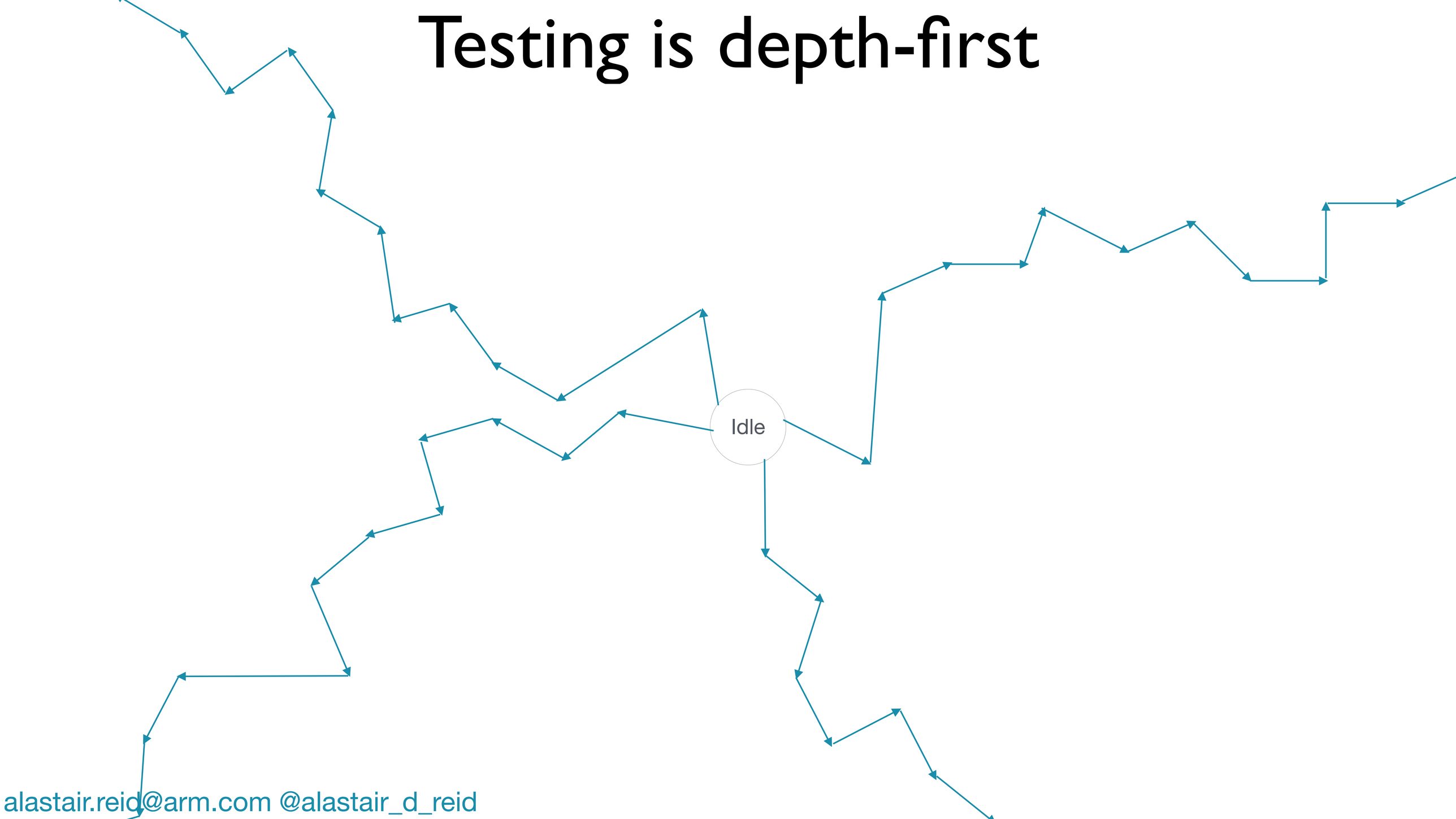

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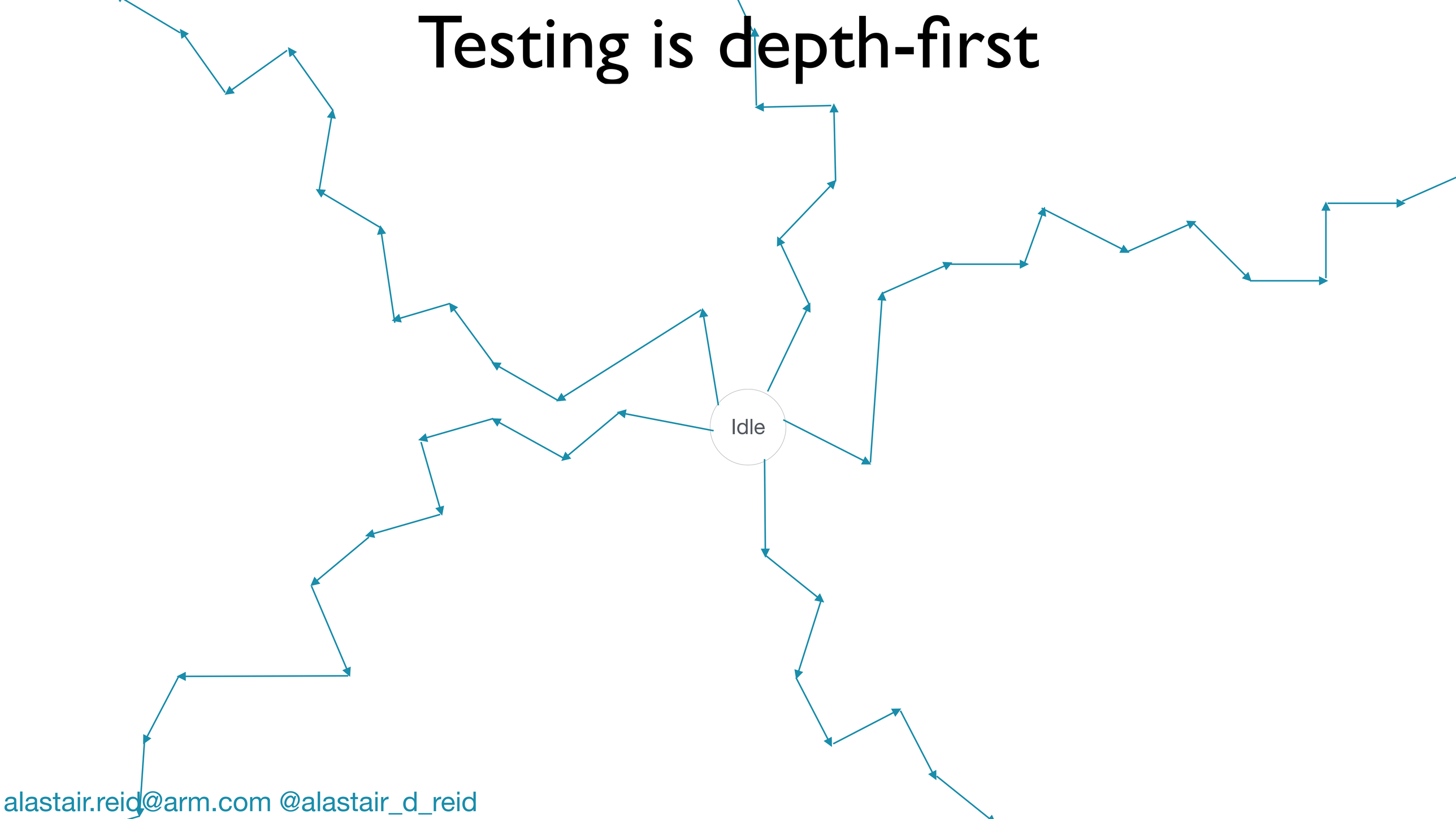

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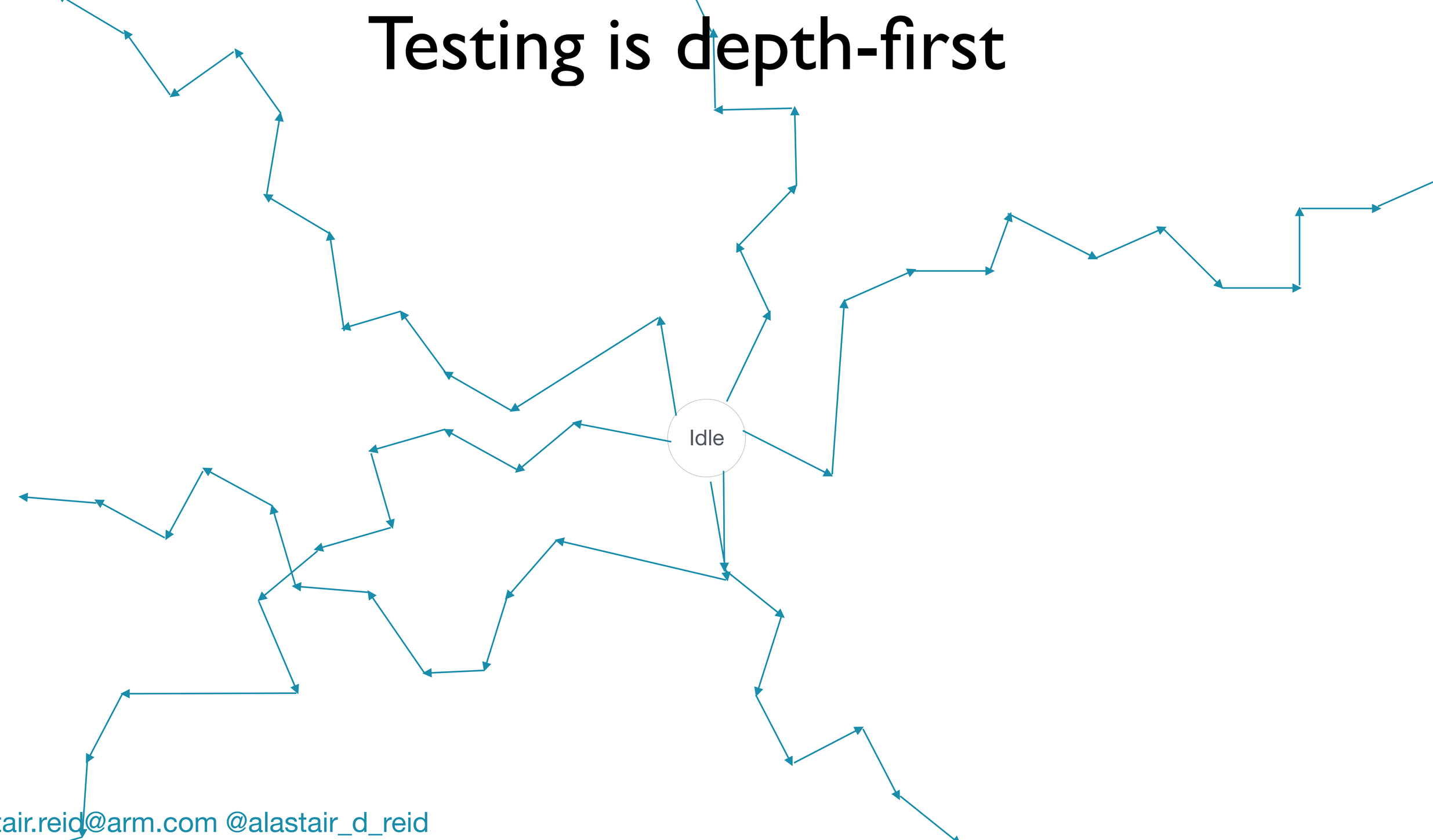

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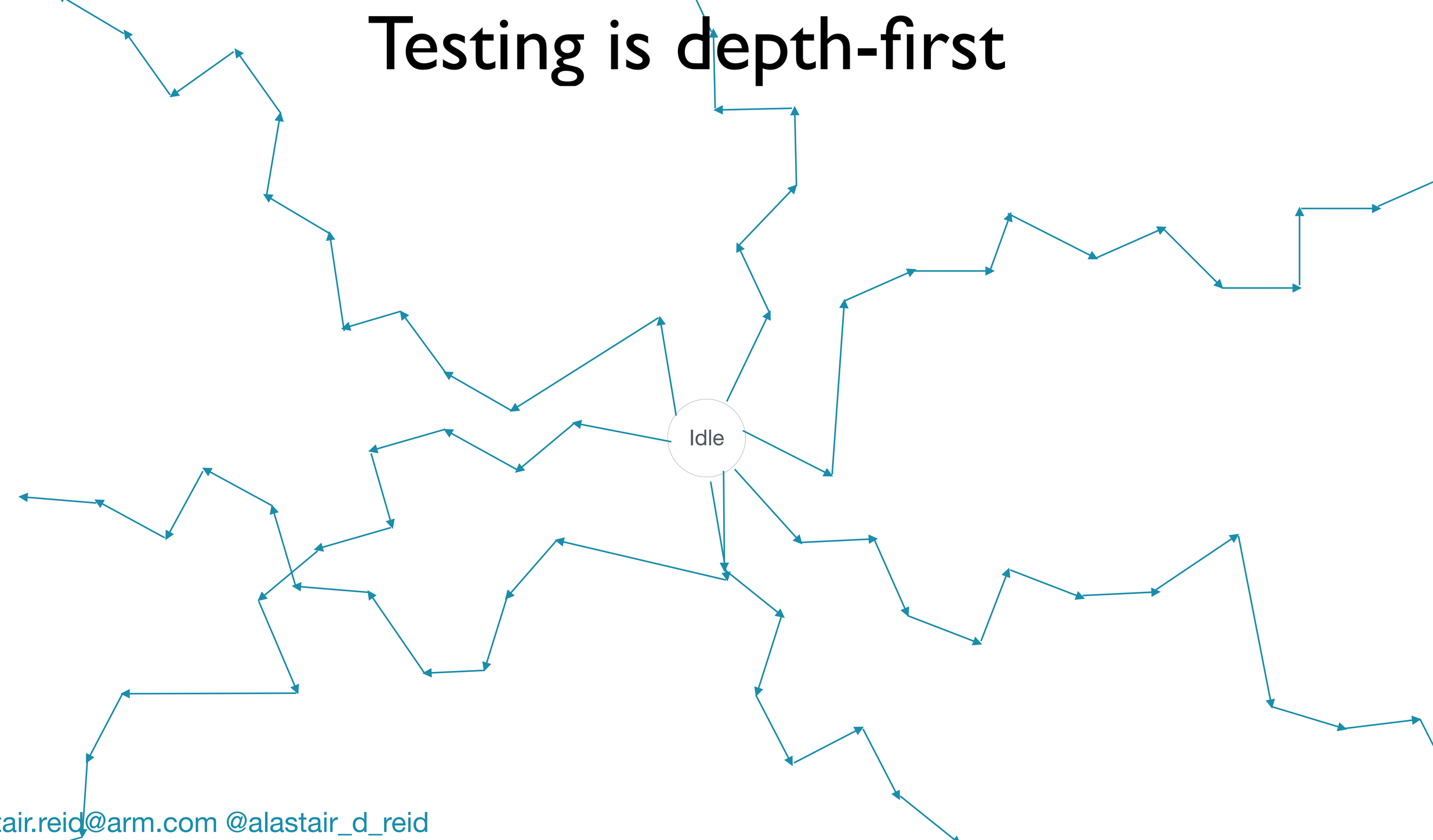

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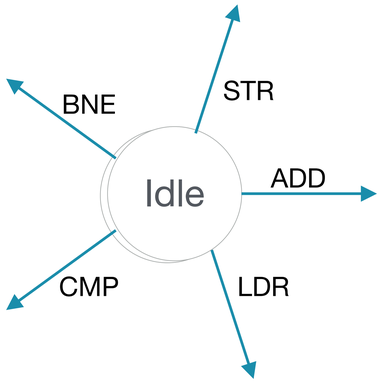

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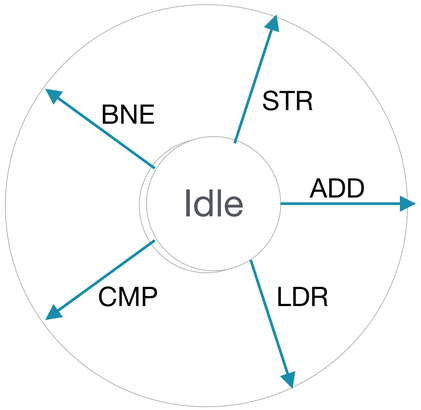

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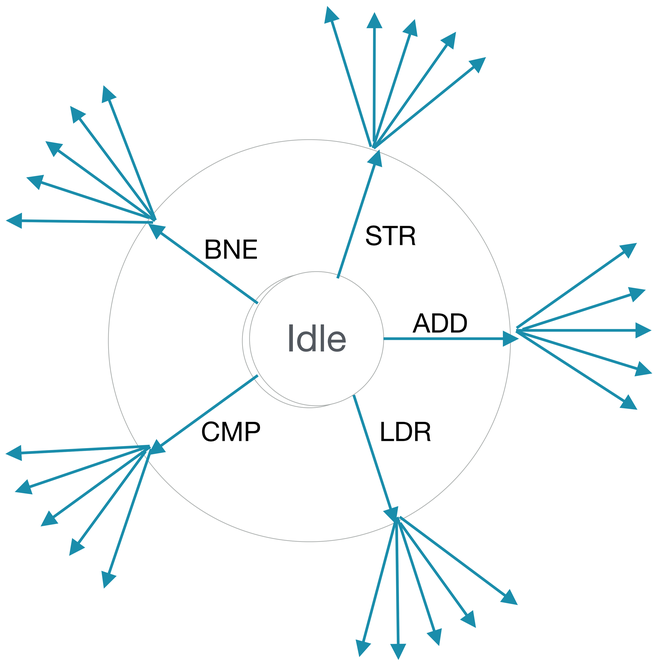

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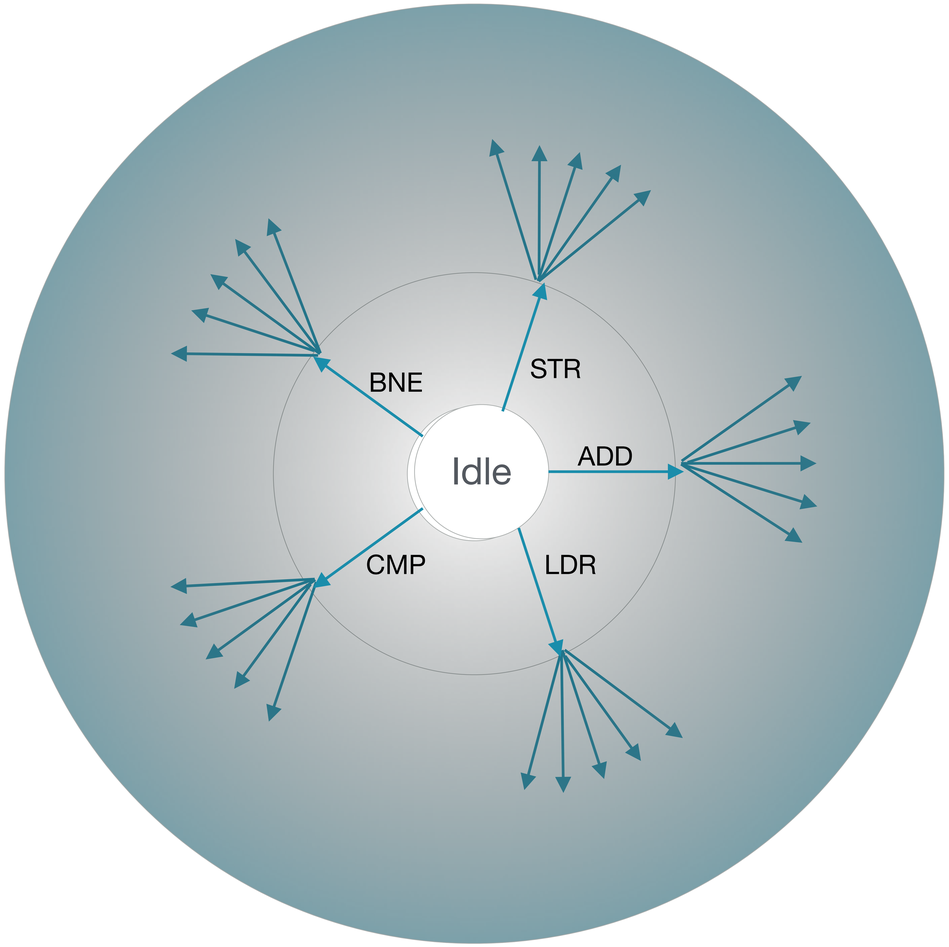

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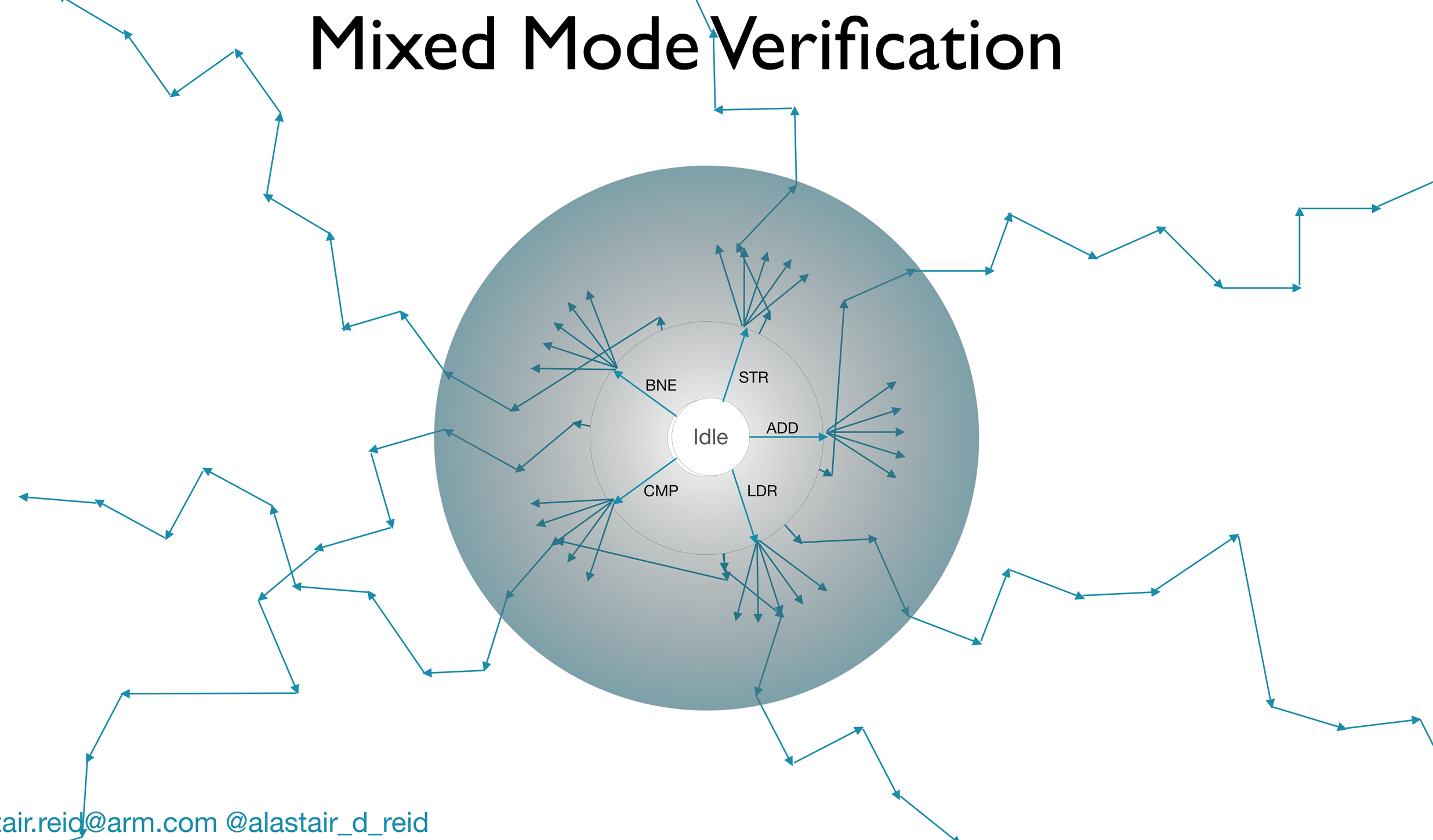

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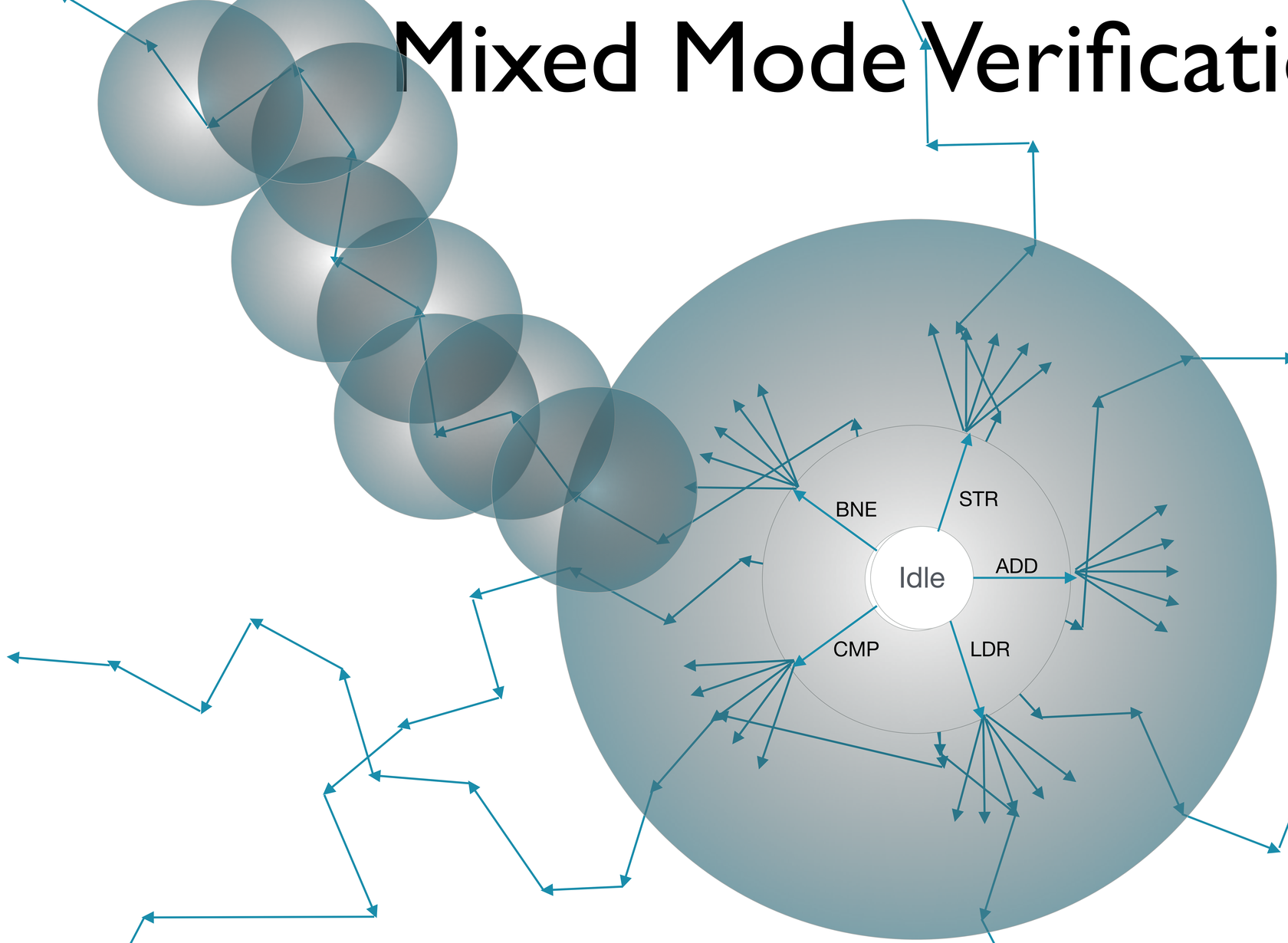

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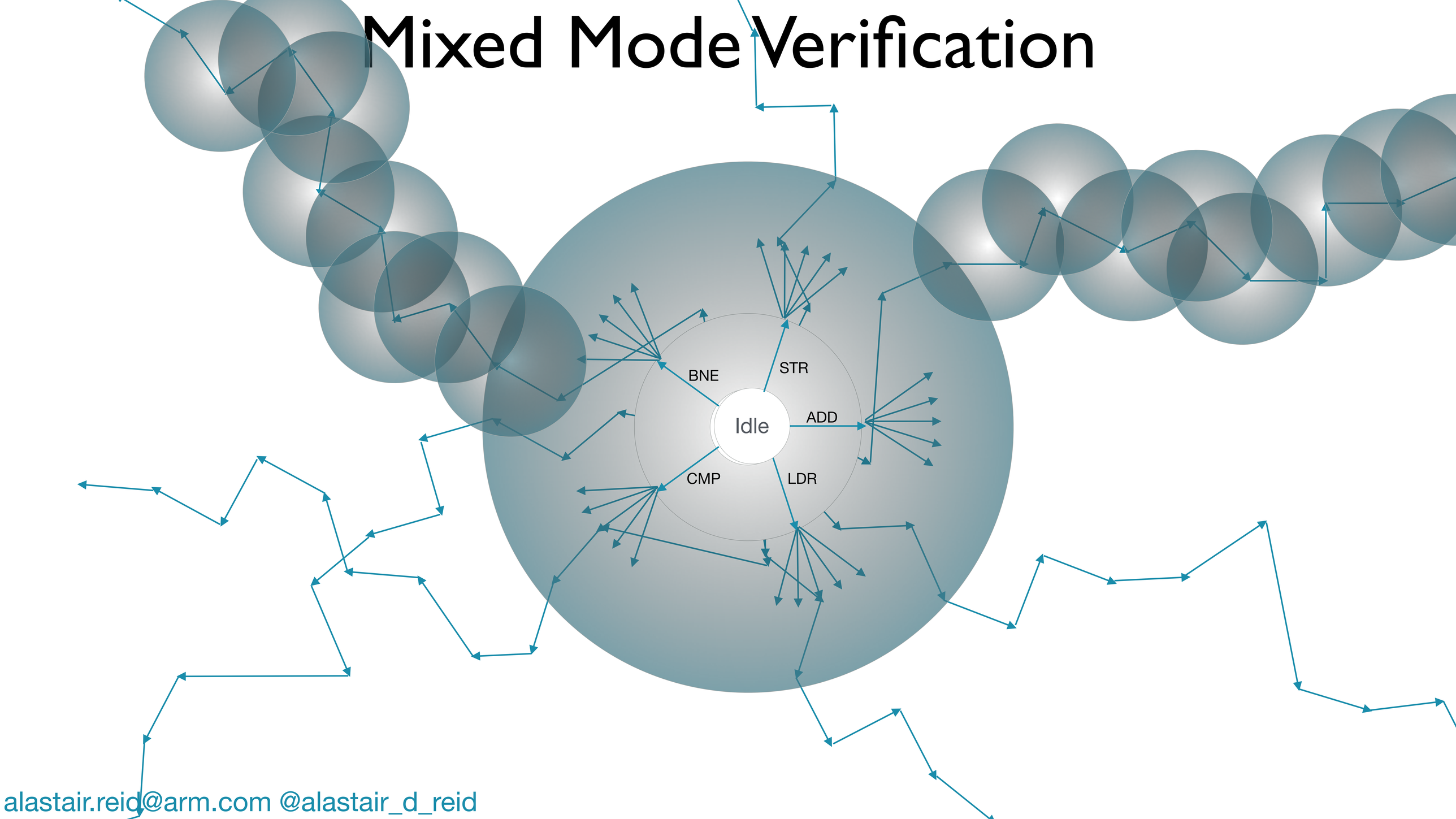

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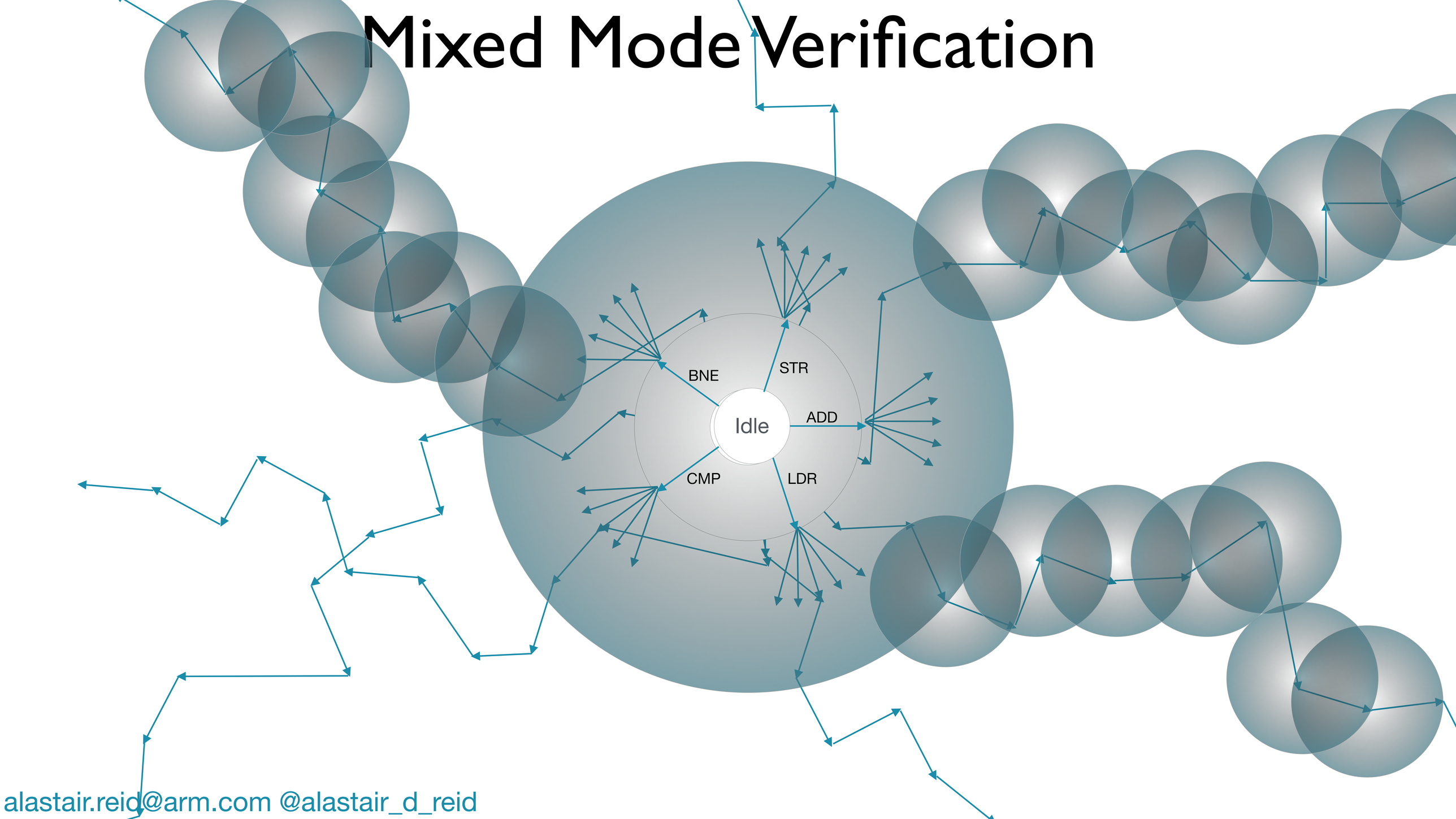

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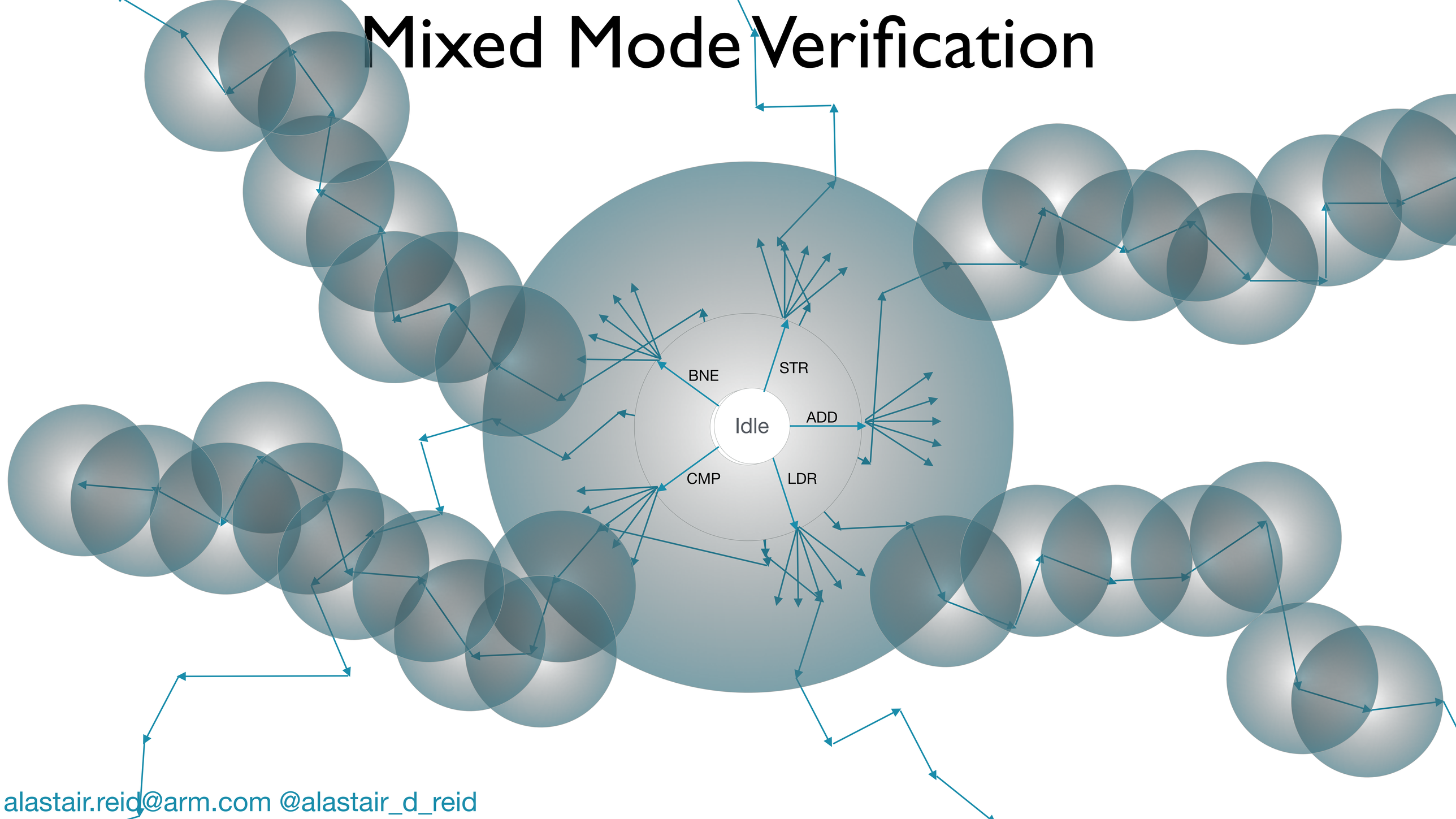

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